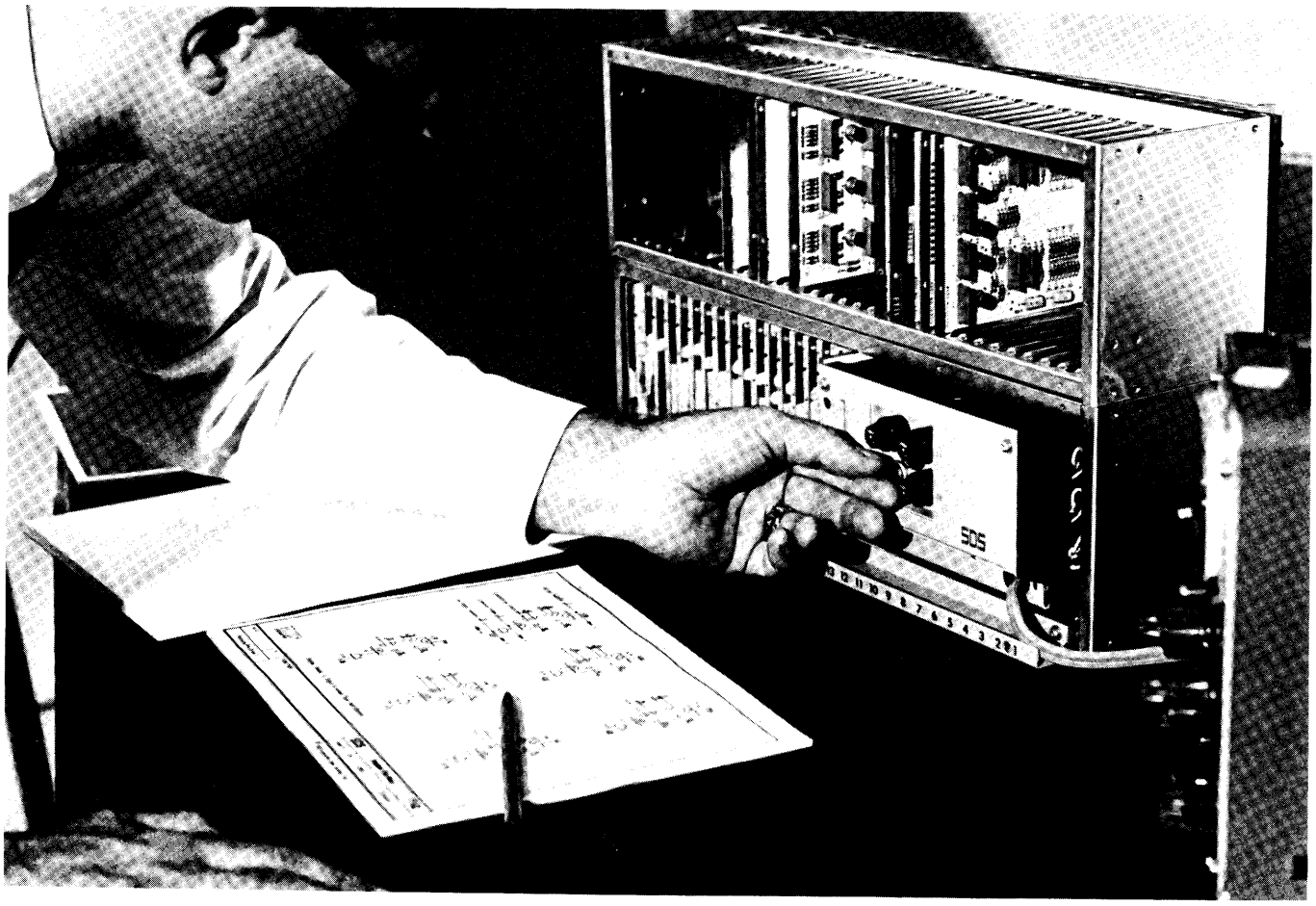
XDS

Xerox Data Systems

IC DIGITAL LOGIC MODULES

T Series
Description and Specifications

Revision 5
September 1969


SDS

SDS T SERIES Integrated Circuit Logic Modules

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THE SDS APPROACH TO MODULES

Logic modules offered by Scientific Data Systems are designed by experienced circuit engineers for system applications. The T Series modules were originally designed for use in the successful SDS Sigma Series general purpose computers, peripherals, and related special-purpose systems.

Since 1961, in the short span of eight years, SDS has produced more than three million modules for use in over 1200 computer based standard and special SDS systems. The first commercial computer with all silicon semiconductors ever delivered by any manufacturer was the SDS 910, shipped in 1962. The first computer with monolithic integrated circuits was the SDS 92, shipped in March 1965. SDS logic modules are in part responsible for the excellent reputation these computers have established for high reliability, flexibility, and low cost.

Now SDS offers its new T Series integrated circuits module family, as used in the Sigma 7, Sigma 5, and Sigma 2 Computers, to solve your system or special purpose logic problems.

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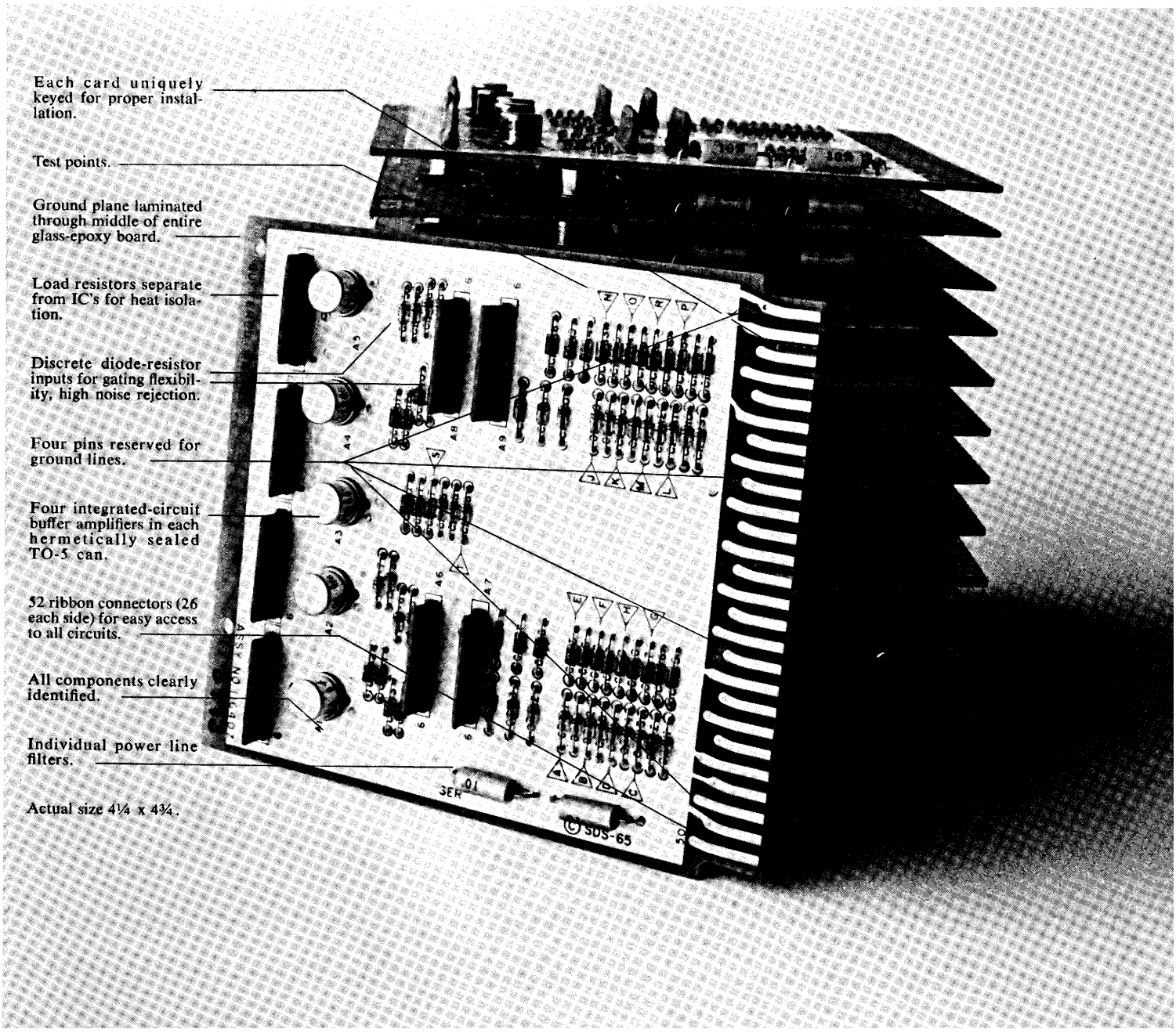
Typical T Series Logic Module



I. INTRODUCTION AND GENERAL SPECIFICATIONS

THIS IS T SERIES:

Experience with the successful SDS Sigma computers has shown that at the present state of component development the best performance, coupled with lower costs, is obtained when monolithic DTL integrated circuit flip-flops, inverters, and buffer amplifiers are combined with close tolerance, discrete diode-resistor gates and output pull-up resistors. Integrated circuits cut costs, save space, improve reliability, and improve performance, by replacing repetitive clusters of transistor circuitry. Diode gates retain flexibility where needed, in the gating structures, and help provide a very high noise rejection of 1.5 volts. Discrete pull-up resistors (load resistors between output collectors and Vcc) allow the use of high current drive by keeping most power dissipation outside the IC package. High current drive makes fan-out large, up to 14 gates per output, and easily permits use of clock frequency up to 10 Mhz because logic line capacitance can be charged rapidly.

Through the use of integrated circuits, 2-stage buffer amplifier cost has been reduced to that of 1-stage inverters. This permits the logic designer to discard the laborious design techniques needed to implement a system entirely with NAND or NOR logic. Logic may now be implemented in a natural way by direct substitution of logic circuits equivalent to the Boolean expressions that appear in the most simplified design equations. This saves both design time and hardware. In T Series these natural logic functions are provided by combining the integrated buffers, inverters, and flip-flops with various combinations of discrete diode-resistor gating. The circuits are grouped on modules in a wide variety of AND, OR, NAND, NOR, AND/OR, and AND/NOR combinations, as described in Section II of this catalog.

A variety of flip-flop modules, with input gating included, are easily assembled into counters and registers. Some are general purpose while others are connected for specialized storage and counting functions. A unique, proprietary monolithic IC flip-flop is used as the storage element. It operates in any of the classic modes: R-S, J-K, T (Toggle), and D (Delay), using less external wiring than is required with the traditional flip-flop design. The clocked set input overrides the clocked reset input when both are simultaneously True, which simplifies input logic and wiring in most cases. Another significant improvement is trailing edge triggering, which reduces the input settling time required as compared to the traditional clocking techniques. The flip-flop also has unclocked inputs for clearing or presetting between clock times, and its outputs are fully buffered to prevent feedback from output lines to inputs.

An economical high-speed IC memory module stores 128 bits for bulk storage and input-output buffering.

Many supporting circuits are provided. Interface modules couple T Series logic into other logic systems with either positive or negative logic levels. An adjustable-threshold Schmitt-Trigger circuit accepts input of arbitrary waveshape and converts to logic levels. One-shots provide accurately adjustable delays. Several clock oscillator types provide timing references. Digital-to-analog converters (with reference voltage regulators) provide outputs that can drive recording and display devices or controllers. Cable receivers and drivers transmit logic signals over longer distances. A variety of lamp drivers and display lamps are available for building displays. Relay drivers and relays are also provided, as well as a manual toggle-switch module.

All of these circuits are placed on the same size epoxyglass etched circuit card, 4-1/4 inches high by 4-3/4 inches deep. The card has 52 gold plated connector contacts to maintain circuit accessibility and still provide dense packing.

The cards plug into connectors which have reliable gold plated, spring loaded, bifurcated (2-pronged) contacts. Thirty-two modules can be placed side-by-side in 19-inch wide mounting cases, which are available in a variety of fixed-mount and hinged models having either wire wrap or solder tail back panel pins. Each mounting case incorporates a ground plane for noise immunity, and includes built-in power busses. Ninety-module tilting drawer cases are also offered. Any of the cases can be mounted in one of three types of cabinets which have 19-inch RETMA rails, doors, ac power wiring, swing-out frames, and optional side panels. A 300 cfm blower is available for cooling. An extender card is provided for troubleshooting.

Jumper wire kits, spooled wire, and wiring tools are available to further simplify mechanical assembly. Blank cards and drilled breadboard cards with circuit etch are available.

Two basic power supplies are offered: a compact supply which slides into a mounting case beside the modules, and a high-output supply which mounts on standard 19-inch rails. Both supplies can operate from a variety of input voltages and frequencies, have overvoltage and overload protection, and ±5% output regulation. Analog and large-system supplies are also available.

A complete range of services is available, from consulting engineering on application problems to a wiring service. Complete and accurate documentation is provided on all products. Application bulletins describe the various phases of building a system, from logic design through documentation and fabrication. Reproducible vellum logic sheets are provided for recording the interconnecting wiring and preparing wire lists.

Thus T Series provides all of the components, information, and services required to design and build a very high performance digital system quickly and at reasonable cost.

GENERAL SPECIFICATIONS

ELECTRICAL AND ENVIRONMENTAL

Supply Voltages

+4 volts
+8 volts
-8 volts
} dc, ±10%

Logic Levels

Logic 1: +4 volts nominal;
+3.6 volts to +10 volts acceptable input range to interface with other module series;
+3.6 volts to +4.4 volts maximum output variation.

Logic 0: 0 volts nominal;
+1 volt to -3 volts acceptable input range to interface with other module series;
0 volt to +0.5 volts maximum output variation.

Noise Thresholds

At logic 0: +1.5 volts (greater may trigger True);
At logic 1: +2.5 volts (lower may trigger False).

The above represents a noise rejection of 1.5 volts in either direction.

Loading

1 unit fan-out load is defined as 3.8 ma max., at the conducting logic level (0 volts).

Input Loading: Any logic input applies 1 unit load to the preceding signal source, unless otherwise noted.

Output Loading: Buffer amplifier, inverter amplifier, or one flip-flop output can each drive 14 unit loads. (One flip-flop drives 28 loads, 14 with each output).

When buffer, inverter, or flip-flop outputs are wired together to form a wired logic function (see page 13), each output attached to the node absorbs 2 unit loads due to the additional pull-up resistor placed at the node.

Timing

Stage Delay (circuit delay):

	Typical	Worst-case
Buffered gate:	18 nsec	30 nsec
Flip-flop:	40 nsec	60 nsec

Frequency Range of Clock: dc to 10 Mhz.

Minimum Input Timing Requirements, Typical: Flip-flop dc input (mark or erase) must be True for at least 40 nsec. Flip-flop clocked input (set or reset) must be True for 30 nsec. before clock changes from True to False, 5 nsec. thereafter.

Minimum Clock Duration: Clock must be True for 30 nsec., False for 60 nsec. Triggering takes place on falling edge when clock reaches the +2v (nominal) switching point. Fall time is not critical.

Temperature

Full-Performance Ambient Operating Temperature: $5^{\circ}C$ to $71^{\circ}C$ ($41^{\circ}F$ to $160^{\circ}F$)

Storage Temperature Range: $-55^{\circ}C$ to $+150^{\circ}C$.

MECHANICAL

Card Size and Type

4-1/4 inches by 4-3/4 inches, epoxy-glass, gold plated etched copper wiring and connector contacts.

Connectors

52 gold-plated etched copper contacts mating with spring-loaded bifurcated (dual prong) connectors. Contacts are 0.15 inches apart; cards are spaced 0.50 inches center to center. Keys prevent wrong insertion.

Back Panel and Wiring

Terminations for wire-wrap, solderless push-on, or solder-tail connection feed through epoxy-glass back panel which is covered with solder plated etched copper ground plane for high frequency shielding. Four terminals from each card position are soldered to ground plane. Power connections are made to etched circuit busses on back panel, soldered to appropriate connector terminals at each card position. Recommended Wire: No. 28AWG copper with cut-through resistant insulation (see page 20).

Mounting Cases

19-inches wide by 5-1/4 inches high, fixed or hinged (32 cards); or 90 card tiltable pull-out drawer, 19 inches wide by 8-3/4 inches high. Welded all steel cases have ventilation slots, multiposition mounting hardware, and optional filtered blowers.

MAKE OR BUY?

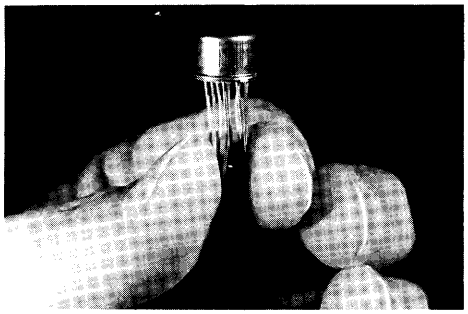
As always, there are cost and performance trade-offs in the decision to make or buy a family of logic modules. In some cases there is an advantage to making modules and buying cabinetry and other supporting components. Usually, however, the costs are greatly underestimated and unexpected performance difficulties arise during checkout, after most of the work has been done and the scheduled time has passed. Many system designers have decided that their time is better spent on system design, and that it pays to take advantage of the module maker's expertise.

SDS offers these benefits with its T Series module family:

1. Exclusive integrated circuits, identical to those used in the SDS Sigma computers, which perform better than commercially available integrated circuits.

2. The advantages of natural logic.

3. Great savings in engineering time. Hundreds of computer systems have been built by SDS using T Series modules. The associated problems in mechanical design, interconnecting wiring design, and manufacturing techniques have been thoroughly worked out and solutions incorporated into the hardware.



4. The components are properly matched in terms of logic mix, loading, frequency response, delay times, noise rejection, power requirements, reliability, environmental specifications, and mechanical compatibility.

5. Supporting circuits, which are particularly subject to unforseen problems, have been designed and refined to properly perform their functions, with adequate safety margins.

6. Special-configuration modules can be built to your specifications at moderate cost.

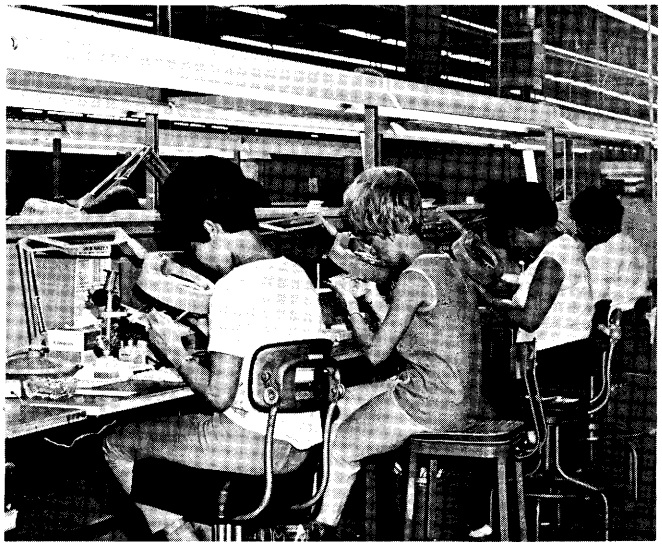
7. Quick delivery. The user receives finished hardware, usually within two weeks or less after receipt of order. Contrast this with the months of manufacturing lead time generally required.

8. Full quality control, of assembled units as well as circuit components. One year warranty against defects. A complete module repair facility is available.

9. Accessories are provided which might be considered too costly in a "make" situation, such as extender cards, jumper wire kits, relay and toggle switch modules, etc.

10. Free application engineering is available, as well as design literature which gives detailed instructions to help avoid mistakes. The products themselves are thoroughly documented.

11. Reproducible logic design and wiring record forms are provided,with complete instructions on their use.



A Portion of The SDS T Series Production Line

Seventy incoming inspection tests can be performed on this T Series monolithic integrated circuit in less than four seconds. The integrated circuit tester is controlled by an SDS 92 computer that accepts or rejects circuits being tested and keeps a record from which engineers can evaluate the quality of circuits supplied by various vendors. Only a large volume module manufacturer can support testing on this scale.

HOW T SERIES MEETS SYSTEM REQUIREMENTS

SYSTEM DESIGN GOALS

Good system design demands high performance at low cost.

In many digital applications, prime PERFORMANCE goals are:

1. Eliminate error (erroneous triggering)
   a. Minimize noise generation or pickup, and reject noise at logic inputs
   b. Maintain accurate timing
   c. Restore attenuated signals to retain signal integrity
2. Achieve fast system speed
   a. Achieve fast rise and fall times on logic levels changes
   b. Minimize propagation delays in logic circuits (stage delay) and interconnections (wiring delay)
   c. Minimize sum of delays in series in each logic chain by reducing the number of elements in series.

The corresponding ECONOMIC goals are:

1. Minimize engineering and related technical labor, particularly when building one-of-a-kind systems.
   a. Design logic simply and rapidly
   b. Plan and document interconnections quickly
   c. Avoid design of special circuits
   d. Assemble system quickly, conveniently, without expensive labor
   e. Debug system quickly
   f. Eliminate callbacks to correct failures
2. Minimize hardware cost
   a. Minimize number of logic elements required to perform a given logic function
   b. Minimize circuit and wiring cost per element
   c. Minimize cabinet hardware required (achieve dense packing)
   d. Minimize cost of other accessories (power supplies, etc.)
   e. Minimize replacement part quantities through standardization
3. Minimize equipment failure
   a. Avoid inconvenient or costly disruption of system operation
   b. Reduce troubleshooting and replacement costs

These goals can be translated into specific hardware design goals. Hardware can be lumped into six broad classes for this analysis (see diagram on page 5). Each group has its own effects on performance and economy. Each will be described in sequence.

GROUP 1. DECISION NETWORKS

Design of gate networks, usually with the aid of Boolean algebra, is often the most time-consuming task. In many cases gates and logic amplifiers also constitute the bulk of the system hardware. Thus, for economy, standard gate-amplifier configurations should be designed to: 1) minimize implementation time, 2) minimize the total number of gates and amplifiers in the system, and 3) cost less per unit.

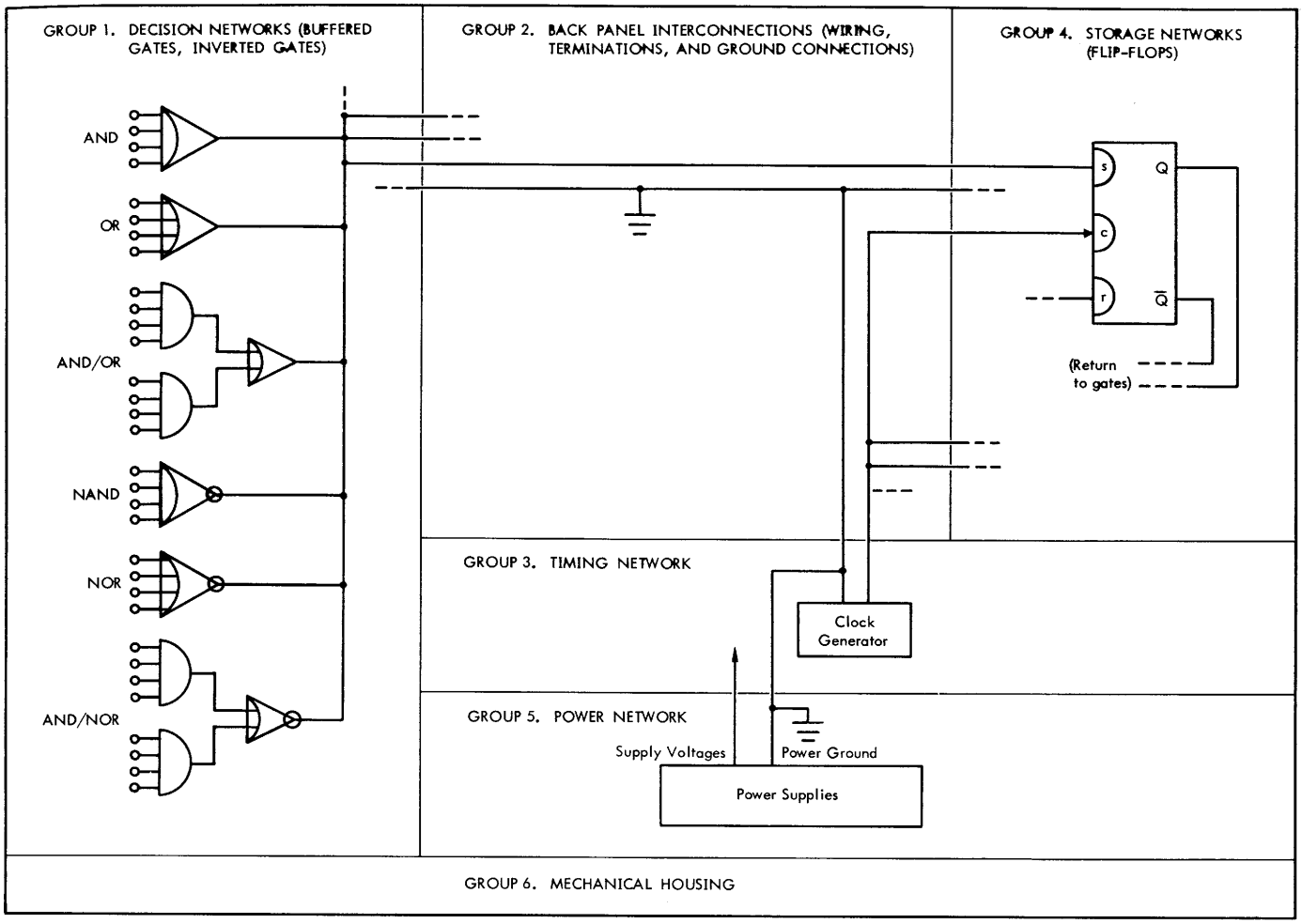
Minimize Implementation Time

The best way to minimize implementation time is to make all four logic functions, AND, OR, NAND, and NOR, available to the designer at the same low cost. T Series does just this. The technique is called natural logic. Once the Boolean expressions that define a logic function have been reduced to simplified form the task is almost finished. The designer then substitutes T Series gating structures directly for equation terms (see Example 1 on page 6).

Many other manufacturers urge the exclusive use of NAND or NOR functions. They standardize on one inverting gate type to solve their problems rather than the user's. But, implementation with only NAND or NOR functions requires additional equation manipulation. T Series eliminates the extra design work by economically providing all four functions. A unique combination of standardized IC logic amplifiers (both inverting and non-inverting) with flexible, discrete diode-resistor gates makes this possible.

SDS logic element modules contain a calculated mix of gate combinations, using gates with 2 to 5 inputs. This selection permits the designer to choose the right combinations of circuits from each card, reducing leftover circuits in the rack and avoiding many wiring problems. The 52 connectors per card permit full access to each circuit.

Load calculations are simple. All T Series logic elements are rated in unit fan-out loads of 3.8 ma. Each diode gate places 1 unit load on the previous amplifier output.



Minimize Hardware Quantity

The number of gates and amplifiers required to implement a given gating function must be the lowest possible.

Amplifiers in particular should be minimized, since they are the active (and therefore expensive) components. Primarily they furnish power to drive logic signals through the gating structure. They also can perform logical inversion, if required. Where adequate power is available, and amplifiers are used merely to perform logic inversions not required by the most simplified form of the equations, they create an inexcusable expense. Example 1 explains how they may be eliminated.

Example 1 also demonstrates another T Series feature that eliminates amplifiers. This is the ability to perform 3-stages of logic (AND-OR-AND) with 1 stage of amplification, without loss of signal quality. The combination of the AND/OR gate with wired-AND functions formed at amplifier outputs makes this possible.

The number of amplifiers is also cut by making output driving current high; this permits each amplifier to drive more gates. The fan-out from a T Series buffer or inverter amplifier is 14 unit loads, compared to 10 for many other types of integrated circuits.

These three T Series features, natural logic, three levels of logic, and high fan-out, typically yield hardware savings of at least 1/3 when compared to other module lines.

Minimize Unit Circuit Costs

SDS T Series achieves low unit circuit costs by integrating the repetitive clusters of components that occur mainly in amplifiers and flip-flops. The number of different integrated circuit types is kept small to simplify design and maintenance. By retaining the inexpensive gate structure outside the integrated circuit, T series retains the flexibility of natural logic. Logic modules (excluding supporting circuits) use only eight different components: 3 integrated circuit types, 3 resistor types, 1 diode type, and 1 decoupling capacitor type. Individual circuit costs are thereby held to a minimum.

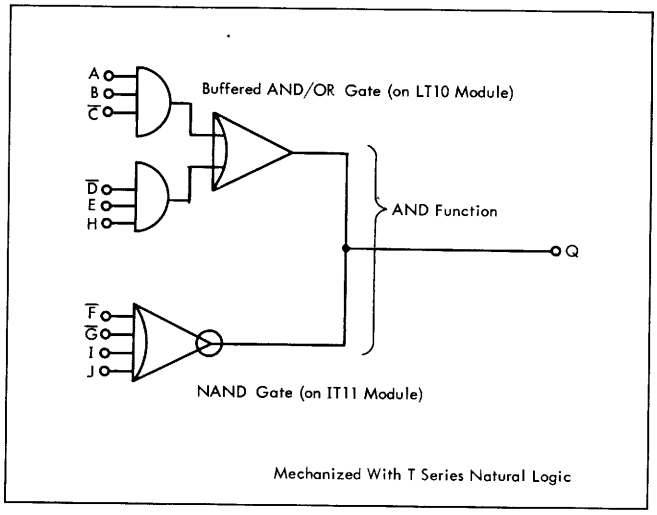
EXAMPLE 1 - NATURAL LOGIC IMPROVES PERFORMANCE AND COSTS LESS

The monolithic integrated buffers, inverters, and flip-flops of T Series are designed to accept inputs from diode AND and OR structures. The unique SDS gating and logic amplifier designs permit three stages of logic to be performed with a single stage of amplification. Any active element such as a non-inverting amplifier may have AND/OR input gates (two stages) and also may have its outputs pararalleled with other active element outputs to implement a third stage of logic.

As an example, mechanize the following function:

$$Q = (AB\overline{C} + \overline{D}EH)\,\overline{(\overline{F}\overline{G}IJ)}$$

T Series natural logic permits direct substitution of hardware for equation terms, as shown below. Note that only two amplifiers are required, one a buffer and one an inverter (NAND).

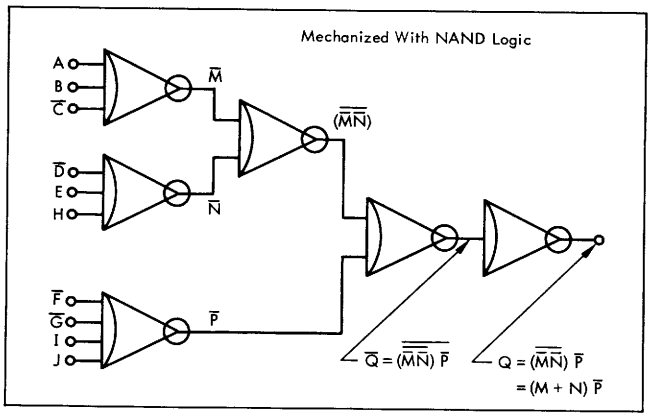


NAND functions are the most commonly available monolithic gate structures offered by other manufacturers. Implementation using NAND functions alone is more complex. First, the equation must be manipulated to represent a series of not-AND operations, of the form $Q = \overline{Y \cdot Z}$, where $Y = \overline{V \cdot X}$, $Z = \overline{T \cdot U}$, etc. As an example let $M = AB\overline{C}$, $N = \overline{D}EH$, and $P = \overline{F}\overline{G}IJ$. By DeMorgan's theorem, the original expression may be rewritten

$$Q = (M + N)\overline{P} = \overline{(\overline{M}\overline{N})}\,\overline{P},$$

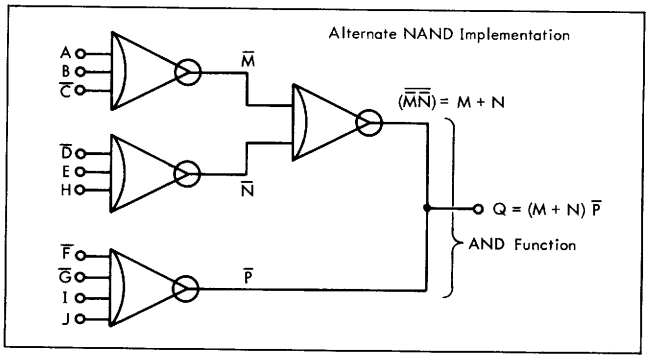
which puts it in the proper form for NAND implementation, providing one more inverter is added since the last NAND gate results in an inversion.

The structure that results using NAND gates is shown in the next column. Note that it uses 6 amplifiers as compared with 2 for the natural logic version.



Mechanizing the same function with NOR gates is similar, but requires 5 amplifiers if all complements are available, or 7 amplifiers if only the given signals are available.

If ANDing at outputs is allowed the implementation is simpler, but still requires 4 logic amplifiers:



For a cost comparison, if we assume that each amplified logic function sells for roughly the same price, then the T Series approach costs 1/2 as much as the best NAND implementation, in this typical example.

To facilitate a comparison of relative delay times, assume that D is the average propagation delay of a diode AND gate or a diode OR gate. Then 5D is a realistic approximation of the delay of an inverting or a non-inverting amplifier. To favor NAND logic, further assume that 5D is also the delay of a monolithic NAND structure. The resulting total delay for the typical circuit illustrated above is 7D with SDS T Series, 20D with straight NAND logic, and 10D with NANDs ANDed at the output.

This example shows how one powerful feature of T Series becomes apparent in a system application. Comparison with other module lines on an individual circuit-for-circuit basis reveals only part of the full merit of T Series modules.

GROUP 2. INTERCONNECTIONS

Sources of Digital System Noise

Digital noise is defined as any unwanted voltage change on the two standard logic levels. Noise can take the form of an internally generated short-duration pulse or a long-duration d-c drift. In addition, there can be pickup of external signals, radiated from nearby devices outside the logic network. Noise introduces error into the data when gating circuits interpret noise as logic changes.

High speed digital systems are particularly subject to pulse-type noise because logic levels change rapidly. All integrated circuits have inherently fast switching speeds, typically in the 5 to 15 nsec range, due to the microscopic scale of the circuits. The ICs will switch at this speed regardless of the system clock frequency. These fast level changes produce high-frequency components which couple readily into the wrong circuits through interwiring capacitance. High speed systems are also sensitive to reflections of leading and trailing edges of pulses. The longer segments of interconnecting wiring act as transmission lines to the high-frequency transient components of logic signals. If these transmission lines are not properly terminated in their characteristic impedances, various reflections can interfere to cause erroneous switching.

The ground system can also create its share of problems at high frequencies. If inductive reactance is high, which often happens when large loops are created by using wires as ground returns, sharp noise pulses may occur at amplifier ground connections, proportional to the product of inductance and switching speed, Ldi/dt.

Another cause of signal degradation is poor contact mesh at the connectors which link the modules to the back panel wiring. Poor mesh or corrosion can lead to intermittent high resistance in logic signal lines.

Minimize Digital System Noise

These problems can be controlled through proper design of the interconnecting wiring and the ground system, and by establishing adequate noise thresholds at the gates. A number of specific objectives are:

1. Prevent inductive or capacitive coupling among back-panel wires. Also prevent coupling between these wires and sources of noise signals external to the system. Design the ground system to have low inductance as well as low resistance.

2. Design the back-panel interconnections to approximate transmission lines in order to achieve characteristics that are independent of frequency. Then terminate these lines (when long) with resistance close to their characteristic impedance, to reduce pulse reflections.

3. Reduce the possibility of poor contact mesh at connectors.

4. Design the gates to have high immunity to noise.

These design goals are all incorporated in T Series.

First, the ground for each module case is a plated flat copper sheet attached to an epoxy-glass board that runs the full width and height of the case. It has very low resistance, and the loops formed by the plane and each interconnecting wire have low inductance, four or five times less than would be the case without a ground plane.

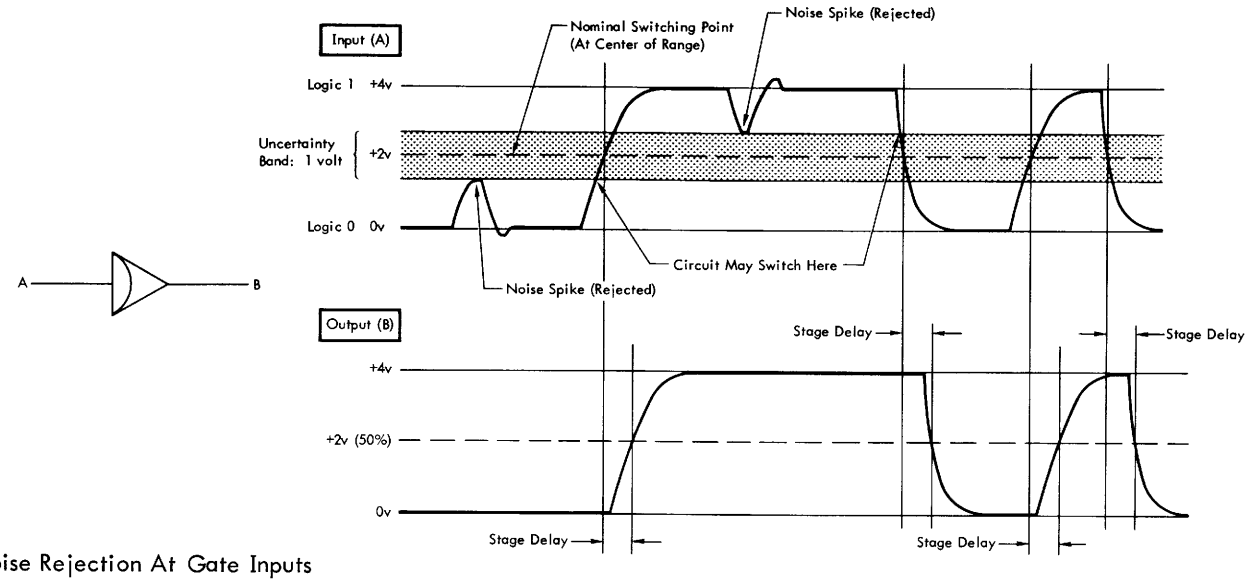
The ground plane is used as a return path for currents in back panel wires. This has the effects of shielding each conductor from each other conductor and of turning each conductor into a transmission line. If the back panel wires are pushed down close to the shield plane the approximate characteristic impedance that results is about 150 ohms.

Second, the terminating impedance at the far end of a long back panel logic signal line may be made to approximate line impedance by connecting a standard 220 ohm terminating resistor, greatly reducing the amplitude of signal reflections. This is possible with T Series because of the high current drive. The discrete terminating resistors (and gate resistors) are outside the integrated circuit container, and power dissipation therefore is not a limiting factor. Signal reflection problems often arise in systems that rely exclusively on monolithic integrated circuits because the integrated load resistances must be considerably larger than line impedance in order to avoid excessive heating of the integrated circuit package.

Third, poor contact mesh is eliminated with the T Series connector design. The connector receptacles for module contacts have one pair of bifurcated (forked conductor), spring loaded, gold plated fingers for each contact. Gold plating reduces the probability of high resistance oxide formation. The fingers are so designed that they cannot distort or lose their spring pressure. Bifurcation provides redundant contacts, further reducing the already remote probability of contact resistance problems. These new connectors are manufactured to SDS specifications.

Wires may be attached to the connector pins (which protrude through openings in the ground plane) with reliable wire-wrap, solder tail, or the new solderless push-on terminals.

The preceding describes the various techniques used to reduce noise. However, since some noise is inevitable, the gates must be able to reject it. The gate switching point is therefore placed at +2 volts and the uncertainty band about this value is made as small as possible through tight component tolerance control.



Noise Rejection At Gate Inputs

Noise Rejection Specifications

With a signal at 0 volts (logic 0 level), noise on a gate input of up to +1.5 volts will not cause the associated amplifier output to change state. With a signal at +4 volts (logic 1 level), noise on a gate input of -1.5 volts, which brings logic 1 voltage down to +2.5 volts, will not cause the associated amplifier output to change state. This leaves an uncertainty band between +1.5 volts and +2.5 volts, within which the amplifier output will switch (see above).

These thresholds are determined by characteristics of the gate diodes, gate resistors, and the integrated amplifier input circuits. The superior noise rejection properties of T Series stem from close tolerance control, and the use of higher, symmetrical noise thresholds.

GROUP 3. SYSTEM TIMING (SPEED)

Propagation Delays and Clock Frequency

Stage delay is the time required for a signal to propagate through a logic circuit. In an idealized sense, it is defined as the time lag between arrival of a step function at a circuit input, and the appearance of a resultant step function at its output.

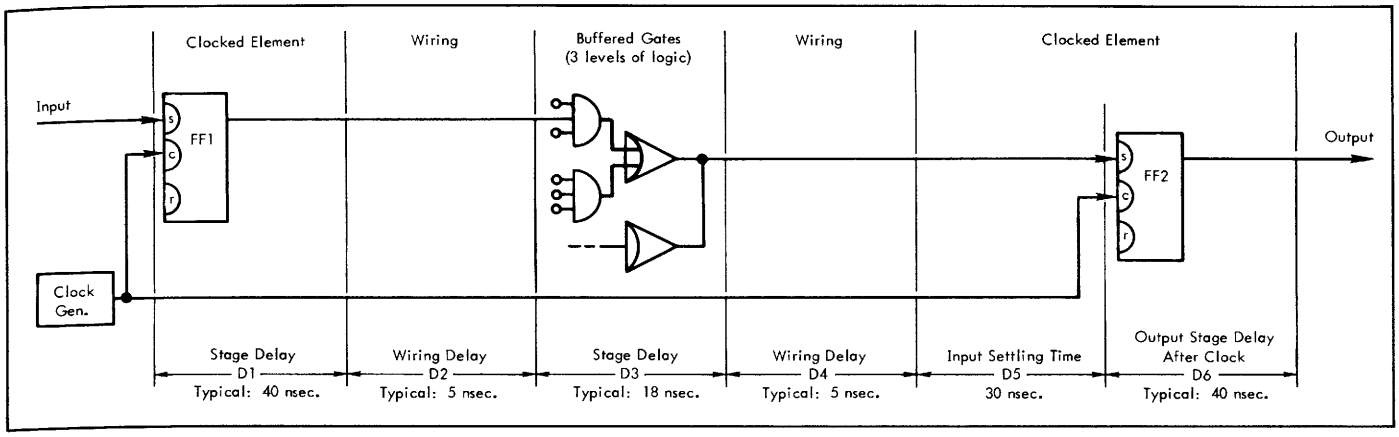
Operating Frequency Range is the repetition rate range of clock pulses over which the clocked system performs reliably in continuous operation while meeting all other specifications.

Since system speed is delay limited it makes no sense to emphasize high clock rate by itself as a desirable feature. A clock oscillator may easily be designed to operate at frequencies unheard of in digital work, but this is no guarantee that a system may be operated at that frequency. The clock must operate slowly enough to permit all logic signals to propagate through an appropriate chain of gates to the next level of flip-flops before the next clock pulse occurs. In other words, the logic circuits must have time to complete their decisions before the clock causes the flip-flops to store the results and commence the next series of logical decisions. Thus to achieve a high clock rate, series delays must be minimized.

The diagram, page 9, illustrates these points. Assume the input is true. When a clock falling edge occurs flip-flop FF1 is set. Its output changes after internal (stage) delay D1. This signal is propagated through a series of wiring paths, gates, and amplifiers with a total delay D2 + D3 + D4, until it reaches another clocked element, FF2. Then FF2 may be triggered by a second clock falling edge after a stabilizing period, D5, and the output is available after an internal delay D6. The clock pulse falling edges, which trigger the flip-flops, cannot be allowed to occur at shorter intervals than the total series delay, D_t = D1 + D2 + D3 + D4 + D5. Thus the maximum permissible clock rate in this example is $1/D_t$. (This has no direct relation to the rate at which a single flip-flop can be toggled).

System design can be varied to some extent to minimize total system delay be performing whole functions in parallel rather than in series. However, the minimum delay in any single chain of elements as illustrated can only be reduced (and clock rate raised) if:

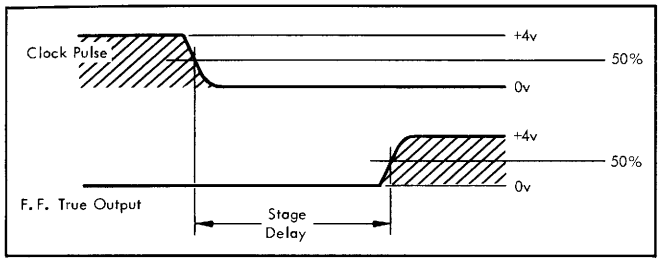
1. Stage delays of flip-flops and amplifiers are minimized
2. Wiring delays are minimized
3. Signal settling time is minimized.



Minimize Active Circuit Delays

The T Series active circuits have very short internal delays. Buffer and inverter amplifiers have stage delays (with input gates included) of 18 nsec. typical, 30 nsec. worst case.

Flip-flop delay is 40 nsec. typical, 60 nsec. worst case, measured as follows:



Minimize Delay Due To Wiring

The stage delays of the active circuits, given above, are measured with the active circuits loaded to permit minimum rise time at the output. In actual practice, when the active circuit output is used to drive a load consisting of back panel wiring and gates, the rise time is extended. This difference in rise time is the delay due to wiring.

The factors which determine delay due to wiring are driver output characteristics, propagation velocity of the wire, length of line driven, and load characteristics. Length of line and load characteristics are the major contributors to wiring delays. Rise time is usually longer than fall time because the driver output presents a high impedance during the 0 to 1 transition, and a low impedance during the 1 to 0 transition.

On the 0 to 1 transition the wiring acts as a capacitance load on the driving circuit; wiring delay thus depends on how fast this capacitance charges. The capacitive characteristic is due not only to stray capacitance, but also to the fact that each wire, which approximates a 150 ohm transmission line, is always loaded with a resistance somewhat greater than its characteristic impedance of 150 ohms, and therefore behaves as a capacitive load. If terminating resistance is decreased to more closely match line impedance, the line behaves more like a resistive load, but fan-out is sacrificed.

Example 2 (on the next page) shows the relations between these factors.

The logic designer has at his disposal the means to trade between fan-out and delay to meet higher speed requirements. He can reduce rise time (at the cost of fan-out) by adding a 5 unit load (220 ohm) terminating resistor to the end of a line, decreasing the RC time constant.

On the 1 to 0 transition the wiring acts generally as an inductive load because the internal impedance of the driving transistor in the conducting condition is very low. As mentioned, this delay is generally less than during the 0 to 1 transition, and is therefore not the limiting factor.

Typical back-panel wiring delays are 5 to 15 nanoseconds when wiring is properly designed.

Minimizing Flip-flop Input Settling Time

A T Series flip-flop set or reset input must be True for at least 30 nanoseconds before clock changes from True to False and stay True for 5 nanoseconds thereafter. This is a relatively short settling time.

Conclusion

The example shown at the top of the page is a typical configuration, having three levels of logic (AND/OR/AND) between clocked elements. The total delay that may be normally expected under these circumstances is obtained by adding the figures given:

$$D_t = D1 + D2 + D3 + D4 + D5$$
$$= 40 + 5 + 18 + 5 + 30 = 98 \text{ nanoseconds.}$$

This allows the use of a clock frequency of $\frac{1}{98 \times 10^{-9}}$

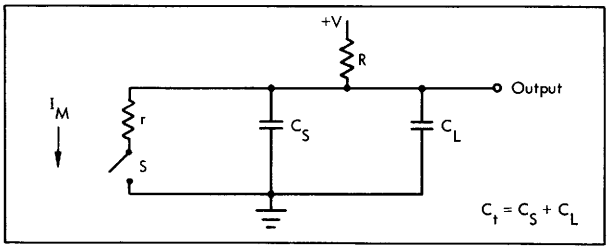
= approximately 10 Mhz.

As can be seen by comparing T Series delay times with those of other module types, the stage delays, the wiring delays, and settling delays are at a minimum. When the design objective is maximum speed, T Series provides the capability to reach clock rates of 10Mhz using normal logic implementation.

EXAMPLE 2 - HIGH CURRENT DRIVE AIDS SYSTEM SPEED

Very high current-handling capability of T Series integrated circuits (up to 60 ma) is directly responsible for two important advantages. One is the exceptionally high fanout of 14 (compared with about 10 offered by other integrated circuit modules). The other is faster system speed.

Shown below is a first approximation schematic of an integrated circuit driving an RC load.



Switch S and small resistance r roughly represent the output transistor of a monolithic gate or flip-flop. Symbol I_M denotes the maximum current handling ability of the output transistor at the 0 level, or fully "on" condition (S closed). Since r typically is small, load resistance R and supply voltage V must be chosen so that current through the transistor in the steady "on" condition does not exceed the limiting value, I_M. Thus with a given supply voltage, V, and a given maximum current handling capability, I_M, $R = V/I_M$.

C_S represents shunt and parasitic capacitance of the transistor. Load capacitance C_L is wiring and pin capacitance to ground, and depends on the length of line driven and the number of connector pins. The total, $C_t = C_S + C_L$.

If the transistor initially is in the "on" condition, with maximum current I_M, output voltage will be nearly zero. If the switch is then opened (transistor cut off), output voltage rises exponentially toward V. The rate of output voltage buildup is controlled by the time constant:

$$RC_t = \frac{V}{I_M} C_t.$$

This equation shows that with a given capacitive loading, the rate of change of voltage on the interconnecting wiring in going from 0 level to 1 level is controlled by the load resistance, and therefore is limited by the ratio of supply voltage to transistor output current handling ability. The lower the supply voltage and the higher the current handling ability, the lower the load resistance (R) that can be used, and therefore the faster the rise times when current is turned off. SDS T Series integrated circuits operate with a relatively low supply voltage and have output transistors with very high output current handling ability, to quickly drive the system through logic level changes.

The real test of any circuit is its speed under load. T Series integrated circuits maintain their high operating speed under conditions of capacitive loading that significantly slow less powerful circuits.

This example is simplified to illustrate the principle involved. In practice, as many as 14 gating circuits are connected across the output. During a 0 to 1 level change each conducting gate supplies 1 unit load of charging current through a pull-up resistor connected to +8v. The supply voltages, load resistance, and pull-up resistances all are chosen so that steady-state current through transistor S does not exceed limiting value I_M. The conclusions of a more detailed analysis are the same: the higher the current handling ability, and the lower the voltages used, the faster the capacitive load can be charged.

GROUP 4. STORAGE NETWORKS

A flip-flop should be both versatile and economical. If possible, it should be designed to minimize interconnecting wiring in the majority of applications. It should have high current output to eliminate the need for amplifiers to drive the next stages of gating.

To enhance system performance the flip-flop should have minimum internal delay, for high speed applications. It should also have a short, precisely timed sampling period (time during which it is sensitive to inputs) in order to avoid erroneous triggering. It must also be insensitive to temperature variations and have excellent long term stability, to prevent erroneous switching due to change in circuit characteristics. Level changes at an output should not feed back through internal cross-coupling to an input, since noise may be present on the output lines.

T Series Flip-Flop Economy Features

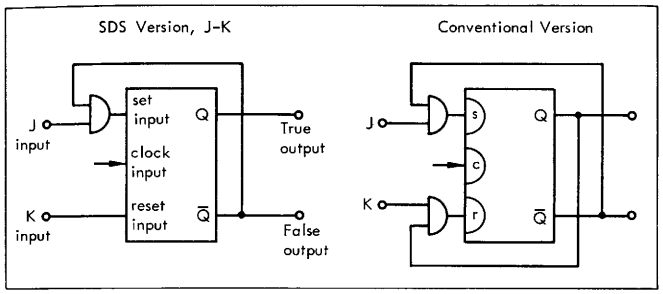
The basic T Series flip-flop achieves these goals. In addition, its outputs can be tied directly to other flip-flop or amplifier outputs to form an AND function without additional gates. This proprietary flip-flop is produced in quantity as a monolithic integrated circuit for low unit cost.

The "set-overrides-reset" feature makes it possible to use one flip-flop with little external wiring in four modes of operation (R-S, J-K, T, and D). A study of systems has revealed that, in the majority of cases, wiring is sim-

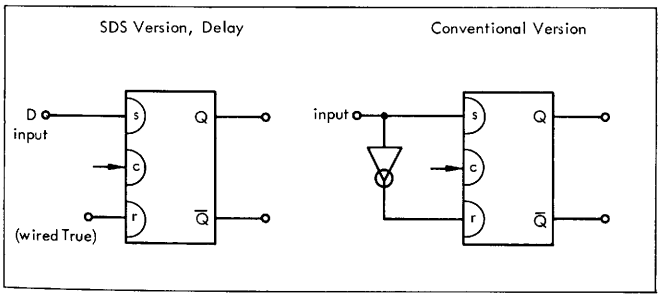
pler if the set input always overrides the reset input when both are True simultaneously:

Period n		n + 1
set input	reset input	Q output
0	0	Same as n
0	1	0
1	0	1
1	1	1

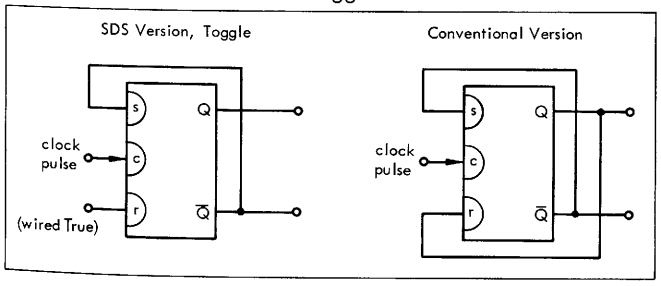
Using this flip-flop, the reset output can be wired to an AND gate at the set input to create a J-K flip-flop. A conventional flip-flop requires a second gate to achieve the same result. The SDS model avoids this second connection because set always overrides reset.



The same feature saves an inverter and reduces wiring in the Delay mode of operation. When the reset input is left open (wired True) the set input operates the circuit as a delay flip-flop--that is, the Q output state follows the set input state, delayed by one clock pulse period.



This feature also saves wiring in the Toggle mode. In this mode the clock input operates the circuit, causing it to change state at each clock trigger.



The flip-flop may also be used as a straight clocked set-reset (R-S) flip-flop with the s and r inputs activated directly, or asynchronously with d-c inputs, mark (m) and erase (e), which override the s and r inputs. Note that in clocked R-S operation there is no ambiguity because set overrides reset.

T Series Flip-Flop Performance Features

The SDS flip-flop has the same fan-out as an amplifier. Each output can drive 14 unit loads.

Internal delay of the basic flip-flop is 40 nanoseconds typical, 60 nanoseconds worst case. Since the minimum clock True time is only 30 nanoseconds a simple toggle circuit such as used in a counter may be operated at a clock rate of 10 Mhz (100 nanoseconds) or faster.

Two features that prevent erroneous switching are a short sampling period and trailing edge clock triggering. Input signal conditions do not affect flip-flop operation, even when the clock input is True, until 30 nsec. prior to the clock's falling edge. The SDS circuit is not the conventional type in which the first rank is set on the 0 to 1 clock input transition, then the state is shifted to the second rank on the 1 to 0 transition. The SDS technique of pure trailing edge triggering provides timing security without undue restrictions on clock pulse shape, and also allows maximum input signal settling time between clocks.

Both flip-flop outputs are buffered within the integrated circuit to completely isolate output signals from inputs.

GROUP 5. POWER

D-c power for logic modules must have low drift. It must also be free from transients, which could cause false triggering. Transients normally enter the system via the a-c power line, particularly when high starting current devices such as motors are on the same line. A module power supply should also be designed to protect the delicate semiconductors from overvoltage or short circuits. Finally, the supply should be capable of being rack mounted and operating with various popular line frequencies and voltages.

T Series Power Supplies

The PT10 (20-40 module supply) and PT12 (125-200 module supply) provide ±5% output regulation, with inputs of either 110 or 230 volts. Both provide overvoltage and short circuit protection. The PT10 plugs into a module mounting case, requiring only 15 module spaces. The PT12 uses the 19-inch rack width.

Power busses for +4v and +8v are supplied on the back plane to minimize high frequency pickup.

Additional transient filtering is provided by individual decoupling circuits on each module.

GROUP 6. MECHANICAL

Mounting hardware should be economical, lightweight, rugged, easy to assembly and disassemble, and compatible with industry standard hardware. It should be available in several options for convenience. Design must take into account electrical properties such as shielding and ground currents as well as heat dissipation.

T Series mounting hardware is based on a standard 19-inch rack width. A welded steel, ventilated 32-module mounting case is available with 2-position front or back bracket mounts, or right/left vertical hinges. A 90-module pull-out drawer is available for high density applications.

Cabinets, blowers, and many other mechanical accessories are also available.

OTHER COST FACTORS

Equipment failure can be costly when it interrupts operation of another system. SDS modules have a proven reliability record. Natural logic results in fewer logic components per system. Integrated circuits reduce the number of wire connection points as much as 20 to 1. All modules are worst case designed and 100% tested. Parts standardization and fewer components per system means smaller, less expensive stocks of replacement parts.

Time consuming special circuit design is avoided because T Series offers many supporting circuit types that SDS engineers have found they need to build a variety of systems, and because special circuit engineering is available at reasonable cost.

SUMMARY

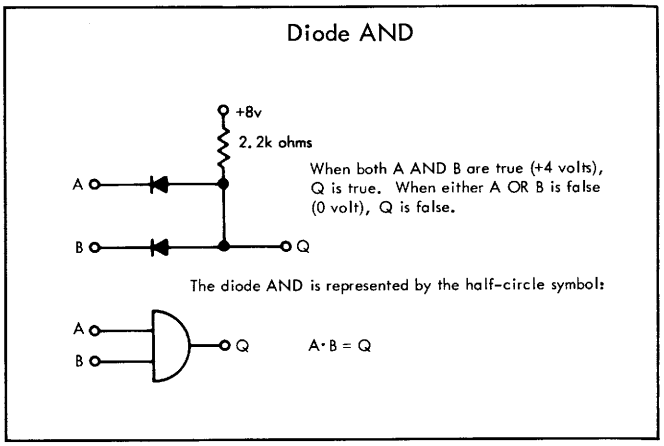
T Series modules are designed for low cost, error-free, high or low speed digital systems that may be assembled quickly, to operate reliably over long periods.

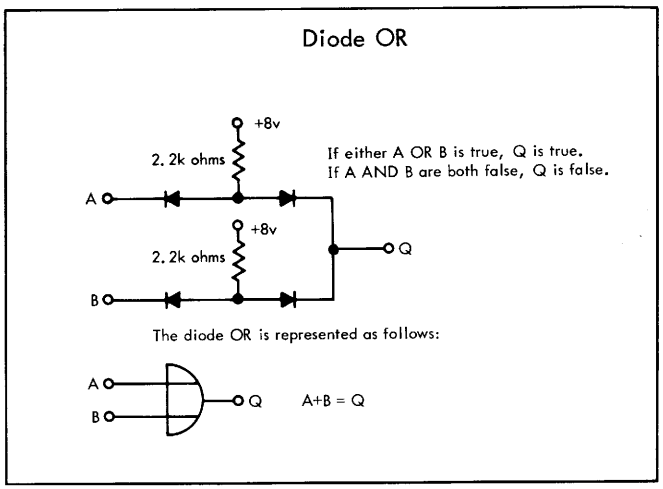
A number of important features such as natural logic, high current drive, back panel ground plane, and set-overrides-reset flip-flop, are unique to the SDS product line. They are responsible for economy and performance benefits.

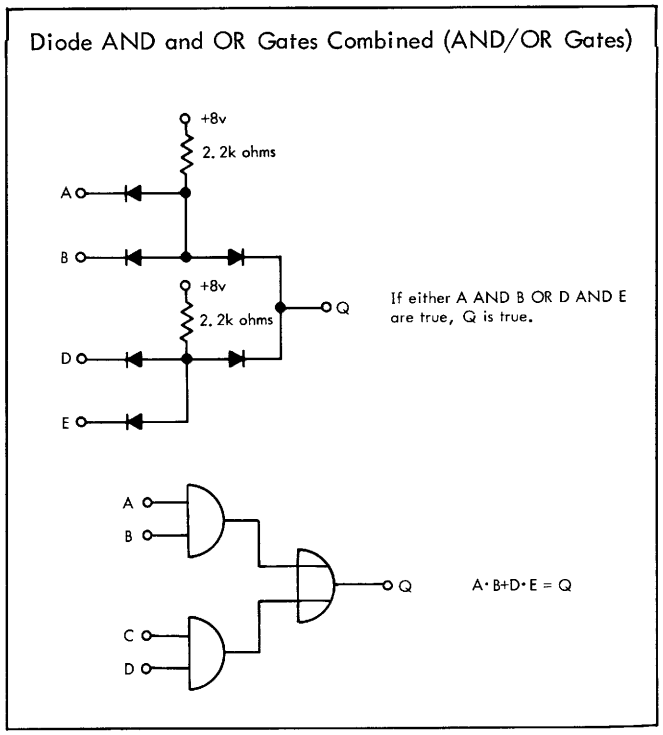
ABOUT THE CIRCUITS . . .

GATES

As mentioned previously, the T Series gating structures are composed of discrete diode-resistor combinations which are external to the integrated circuit buffers, inverters, flip-flops, and other IC elements such as the 8-bit memory circuit used with the FT40 module. Thus the number of different ICs used is very small, but complete gating flexibility is retained, along with better noise rejection. The structure of the AND, OR, and AND/OR gates is shown at right.







LOGIC AMPLIFIERS

In order to preserve good signal characteristics, in T Series logic the output of a diode AND, OR, or an AND/OR combination never serves as input to another stage of diode gate circuits. It is always connected to an active element which restores the signal to the proper power level and filters out random noise. Active elements include inverting amplifiers, non-inverting (buffer) amplifiers, flip-flops and others, usually in IC form. The outputs of these active elements drive other gate inputs.

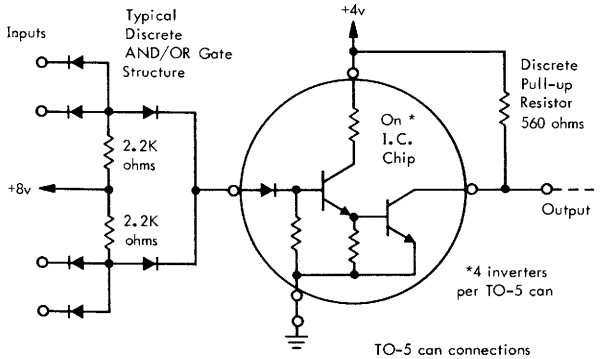
The most basic active elements are the non-inverting logic amplifiers (buffers) which standardize the signal waveshape and provide power gain (fan-out) for driving parallel loads.

The inverting logic amplifiers perform the same driving function plus the additional function of logical negation. The circle shown on the inverter symbol indicates this.

For convenience, buffered or inverted gates are symbolized with combined gate-amplifier symbols as shown on page 21.

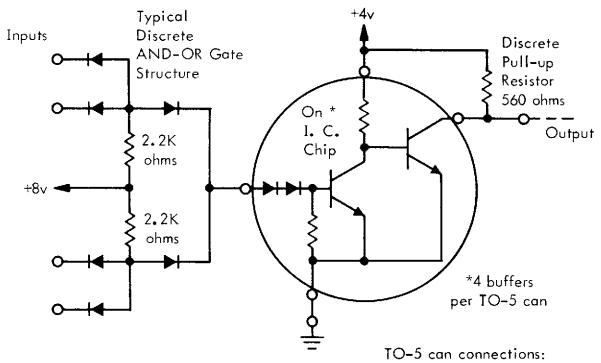
The illustrations below show the essentials of the buffer and inverter circuits, with inputs preceded by a typical discrete AND/OR gate. Note that the logic line pull-up resistors are also kept discrete, to obtain high current drive for fast rise time and high fan-out without reducing reliability by overheating the IC container. This also provides for the possibility of forming wired logic functions (or expanding gate functions) by tying several outputs together with only one pull-up resistor on the line, thereby preserving fan-out for useful loads. The model numbers SDS 305 and SDS 306 refer to the ICs, which contain four buffers or four inverters per one high-reliability TO-5 can.

SDS 305 Inverter Microcircuit



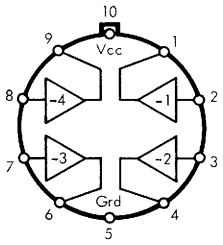
IC Specifications:
- Turn-on delay 20 nsec. max. (50% points)
- Turn-off delay 30 nsec. max. (50% points)
- Typical stage delay: 18 nsec. average
  5 nsec. min. (not guaranteed)
- Output Drive 60 ma (16 Unit Loads)
- Fan-out with 560 ohm pull-up; 14 Unit Loads (pull-up absorbs 2 Unit Loads)

SDS 306 Buffer Microcircuit



IC Specifications:
- Turn-on delay 25 nsec. max. (50% points)
- Turn-off delay 25 nsec. max. (50% points)
- Typical stage delay: 18 nsec. average
  5 nsec. min. (not guaranteed)
- Output Drive 60 ma (16 Unit Loads)
- Fan-out with 560 ohm pull-up; 14 Unit Loads (pull-up absorbs 2 Unit Loads)

TO-5 can connections:

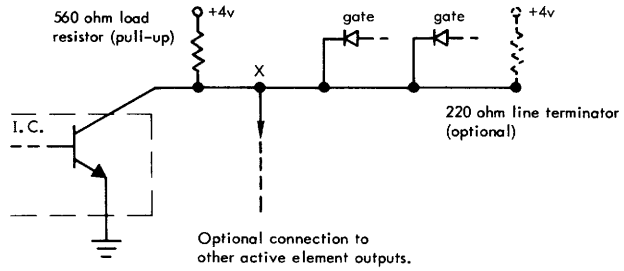


WIRED-OUTPUT GATES

With T Series it is possible to form gate functions by wiring buffer or inverter outputs together, thus creating a new gate function without additional hardware.

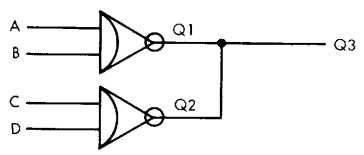
T Series logic outputs are normally constructed as shown below. When outputs are connected at point X an AND function is formed, as follows: when an integrated circuit output transistor conducts it shorts the logic line to ground, placing the line at logic 0. This is an AND function because all outputs must be at logic 1 for the line to be at logic 1.

Standard T Series output connected to logic line:



If all outputs are inverter outputs the wired gate can be considered a NOR as shown below.

Wired NOR



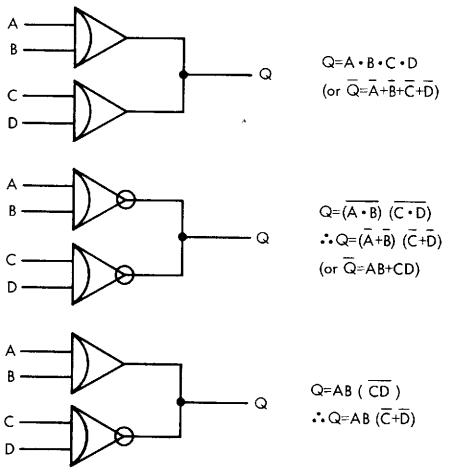
Output Q1 = $\overline{A \cdot B}$, and output Q2 = $\overline{C \cdot D}$. By connecting Q1 and Q2 an AND function is formed, Q3 = $(\overline{A \cdot B})\,(\overline{C \cdot D})$. By DeMorgan's theorem, this is equivalent to

$$Q3 = \overline{(A \cdot B) + (C \cdot D)}$$

which is a NOR function because it has the form $Q = \overline{X + Y}$ (where $X = A \cdot B$, $Y = C \cdot D$).

The basic wired functions that can be formed with two outputs are given below. Up to seven outputs, each having a 560 ohm pull-up, may be wired together.

Wired-output Gates



The trade-off for this additional logic capability is a reduction of fan-out. Each additional output absorbs 2 unit loads due to the additional 560 ohm pull-up resistor that is placed in parallel at the node. No more than seven outputs can be connected since seven pull-ups absorb 14 unit loads, leaving 2 unit loads for useful output.

However, if the additional pull-up resistors were not present there would be no fan-out reduction due to loading. Then the upper limit of fan-out is determined by the drop across the pull-up, which decreases noise margin in the True state. A 560 ohm pull-up can handle 6 common outputs; 220 ohms can handle 16. On some modules the pull-up is omitted to permit this (see IT14 module description).

The wired-output technique also allows gate expansion (increase of fan-in). For instance, four 2-input NORs can be wired together at their outputs to form one 8-input NOR.

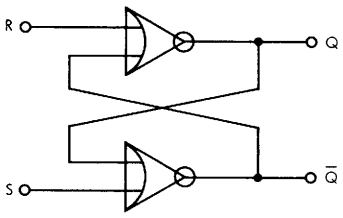
STORAGE ELEMENTS

The results of the decisions made by gates can be stored in one of several devices. All of them have two stable states, and when implemented with ICs or transistors are called flip-flops.

Dc Flip-Flop

A simple dc flip-flop made by cross-coupling two buffered NOR gates (inverted ORs) stores 1 bit. It has the disadvantage that inputs are sensitive to changes on the output logic lines because the outputs are directly fed back to the inputs without intervening buffers to isolate them. However, in a suitable application the dc flip-flop reduces storage cost. When the S input is made True (and R is False) the unit assumes one state (Q True, $\overline{Q}$ False) and retains this state after S becomes False due to the feedback from Q. The opposite conditions flip the unit to the opposite stable state. When both inputs are made True simultaneously the state is indeterminate, and if the True level on both inputs is removed simultaneously the state is indeterminate. However, if one True level is removed before the other, and the one remaining is held True for the duration of the circuit delay of the logic amplifiers (30 nsec worst case) then the unit assumes the state determined by the last True input.

Simple dc flip-flop, using two gated SDS 305 ICs



$Q = S\bar{R}$, $\bar{Q} = R\bar{S}$ (See FT57 description)

Clocked Flip-Flop

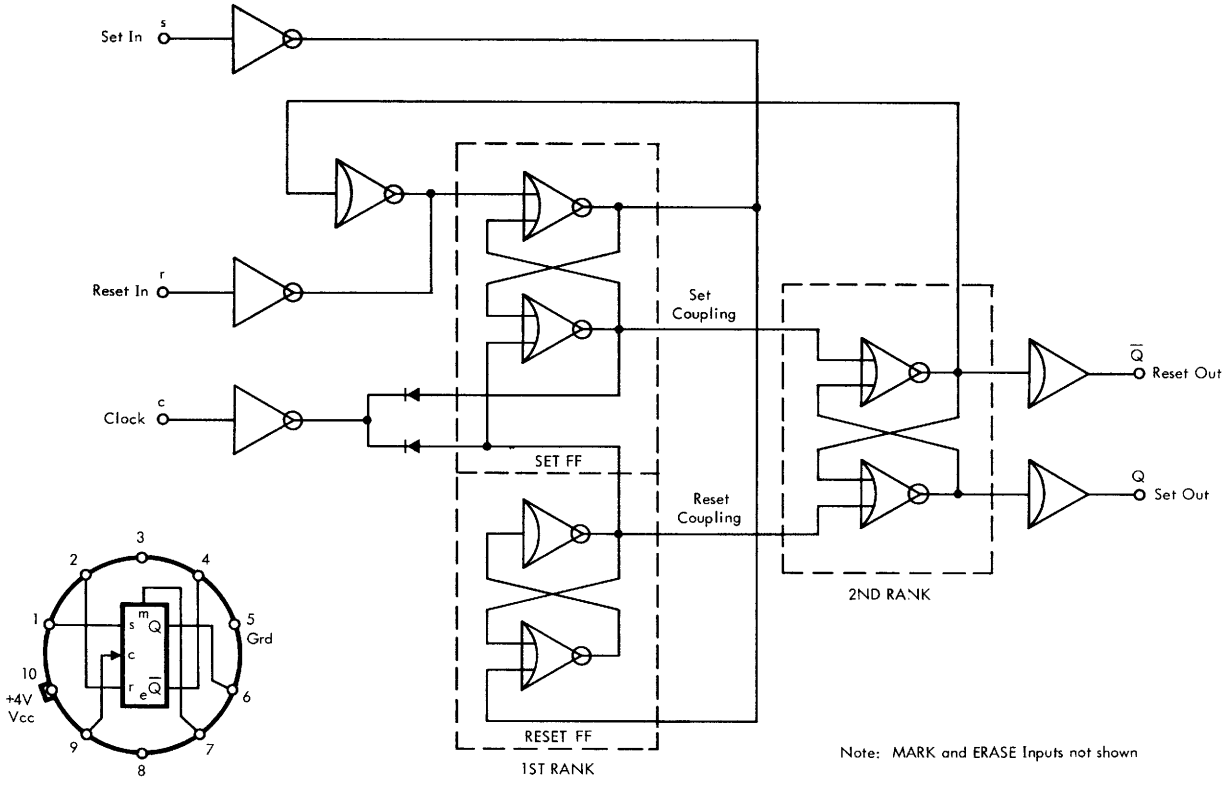
A more sophisticated flip-flop is used for most storage applications. Its cost is only slightly higher than that of the simple dc flip-flop because the entire circuit is placed on a single IC chip. This flip-flop IC is designated the SDS 307. Its characteristics are described in the diagram on page 15.

As can be seen from the logic diagram of the IC, the flip-flop is essentially a structure of NOR elements, but much more complex than the simple dc flip-flop described previously.

The flip-flop has a pair of dc inputs (called mark for dc set and erase for dc reset) which can be used to make the flip-flop behave like the simple dc flip-flop described before. Their primary use is to override the clocked set and reset (s and r) inputs, so that the flip-flop can be preset or cleared between clock trailing edges.

IC Specifications:

Clock requirements:	30 nsec. min. True (50% points). 60 nsec. min. False (50% points). 1 Unit Load, standard logic signal.
Set and reset inputs:	Must be stable from 30 nsec. min. before clock trailing edge to 5 nsec. min. after clock trailing edge. Flip-flop is insensitive to these inputs at other times. Require 1 Unit Load each.
Mark and erase inputs:	40 nsec. min. True on mark input to set flip-flop; 40 nsec. min. True on erase input to reset flip-flop. Require 1 Unit Load each.
Output timing:	15 nsec. min. after clock trailing edge (50% points); 60 nsec. max. after clock trailing edge (50% points); 60 nsec. max. after mark-erase leading edge (50% points).
Output Isolation:	Completely buffered (cannot alter internal flip-flop state by output collector grounding).
Output drive:	Fan-out of 16 Unit loads maximum from Q output; 16 from $\overline{Q}$ output. When 560 ohm pull-up resistors are used, fan-out is reduced to 14 Unit loads.
Circuit components:	IC contains 28 transistors, 36 resistors, and 10 diodes.



TO-5 Can Connections

Internal Logic Diagram

SDS 307 High Speed Flip-flop Microcircuit

When the mark input becomes True, the Q output becomes True and stays True regardless of the state of the mark input, and the $\overline{Q}$ output becomes False. When the erase input becomes True, the $\overline{Q}$ output becomes True and stays True and the Q output becomes False. If both dc inputs become True simultaneously, both outputs will become False as long as both inputs are held True. If one input then becomes False the flip-flop assumes the state determined by the other input, providing it remains True at least 40 nsec.

The gating to the flip-flop inputs is external to the IC, just as with buffers and inverters. The output pull-up resistor is also external to the chip. Gates are placed on the module; therefore, the IC inputs are not directly accessible at the module connector. On many modules the reset (r) inputs are wired True. That is, they are connected via circuit etch through a resistor to +8 volts. This eliminates external wiring to the r input in many applications. It is possible to wire the SDS flip-flop in this unique way because a True signal on the set (s) input always overrides a True on the reset (r) input.

The set-override mechanism and the other SDS 307 features can be understood in terms of the IC logic diagram above. The flip-flop is a dual rank configuration of NOR elements. The second rank is a simple NOR flip-flop, coupled to the output pins through buffers that each provide 60 ma (16 unit loads), normally connected to external pull-ups. The first rank consists of two flip-flops, one for set and one for reset. The two internal lines which couple the first rank to the second also connect to the clock inverter. When the clock goes True these two lines are clamped to ground, isolating the second rank so that it holds its original state. During this time, while clock is True, the set and reset flip-flops are primed to the states of their inputs. When clock falls they assume the new states and regain control of the second rank flip-flop. Note that the outputs change to the new state on the clock trailing edge. Inputs must be steady for 30 nsec preceding and 5 nsec following the clock trailing edge to permit first rank flip-flops to stabilize.

The set inverter will always override inputs to the reset inverter when the set input is True because it is coupled to an output of the set flip-flop, forming a wired AND, while the reset inverter is coupled to an input. This is the basis for the set-override feature.

The second rank output is fed back to the first rank so that the outputs remain unchanged when clock pulses occur with both set and reset inputs False.

Note that the mark and erase inputs are not shown in the diagram. Essentially they bypass the first rank, activating the second rank directly, thus overriding the entire set-reset-clock structure.

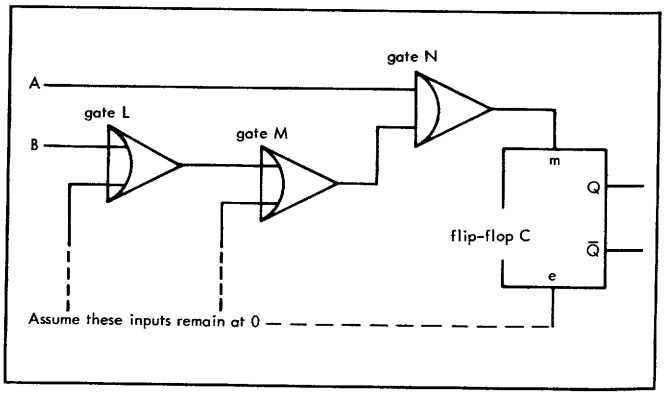
Advantages Of Clocked Flip-flop Operation

The use of a clock, or system time reference, was briefly mentioned in the discussion of system requirements, and will be reviewed in more detail here.

A clock pulse, which is a logic signal that is sent simultaneously to all flip-flops in a synchronous system, serves to inhibit storage of logic signals during the periods when changes are taking place on the logic lines (the etched circuit and back-panel wiring that connects all inputs and outputs). The clock accomplishes this by limiting the time that new information can be stored in a clocked flip-flop via the set and reset inputs to the short duration (usually 5 to 10 nanoseconds) of the clock trailing edge. While the clock is high the second rank flip-flop of the SDS 307 retains its original state. It is only when the clock level falls that the state of the first rank flip-flops is transferred to the second. Then, while the clock level is False, the set and reset outputs remain as they are. The latter can be verified by assuming the several s and r input possibilities and working through the logic diagram.

The use of the clock avoids timing problems due to logic race conditions which can result when level changes arrive at flip-flop inputs at different times, because of different propagation delays in the electrical components in parallel paths leading to the same flip-flop. A logic race condition is present when one signal causes a flip-flop to change state before all signals have had time to settle to their final levels.

As an illustration, consider the simple network shown below, which uses the mark and erase inputs to illustrate the operation of a flip-flop without a clock. Assume that flip-flop C is initially in the reset condition. Also assume that level A is initially False while level B is initially True. Now if A becomes True and simultaneously B becomes False, the new value of A arrives at gate N before the new value of B arrives, because the B change is delayed in going through gates L and M. Therefore, both inputs to gate N are True for the duration of the delay. Since the mark input of C is at all times sensitive to the output of gate N, flip-flop C will erroneously set if the delay is long enough. When the new value of B finally arrives at gate N, the desired input condition to flip-flop C is established, but an incorrect result has already been stored in C and cannot be reversed.



Obviously the problem is avoided if the output of gate N is not allowed to change flip-flop C state until after all signals have settled. The trailing edge trigger clock technique provides the longest possible settling time.

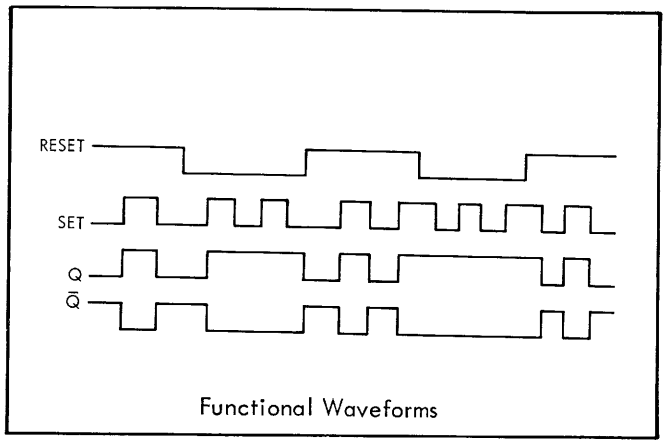
Buffered Latch

Another storage element used in T Series modules is the SDS 309 Buffered Latch microcircuit. This microcircuit provides the storage capabilities of a DC flip-flop and at the same time eliminates noise-induced delatching which sometimes affects other types of latch circuits.

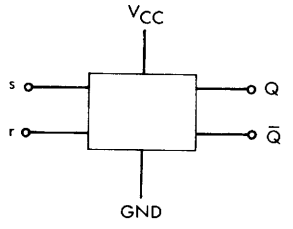
One TO-96 case contains two buffered latch circuits. The logic symbol, pin connections, and schematic representation of a buffered latch are given in the figure below.

The buffered latch circuit has two modes of operation. One mode is defined by the reset input (r) being true (1), the other mode is defined by r being false (0). The functional waveforms in the figure shown at right support the following explanation of the two modes of operation.

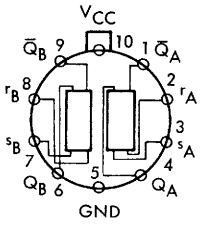
If the reset input (r) is true (1), then the output (Q) follows the set input (s). If the reset input (r) is false (0), then the output (Q) will go true (1) with the first occurrence of a set pulse and remain true so long as the reset input (r) remains false.



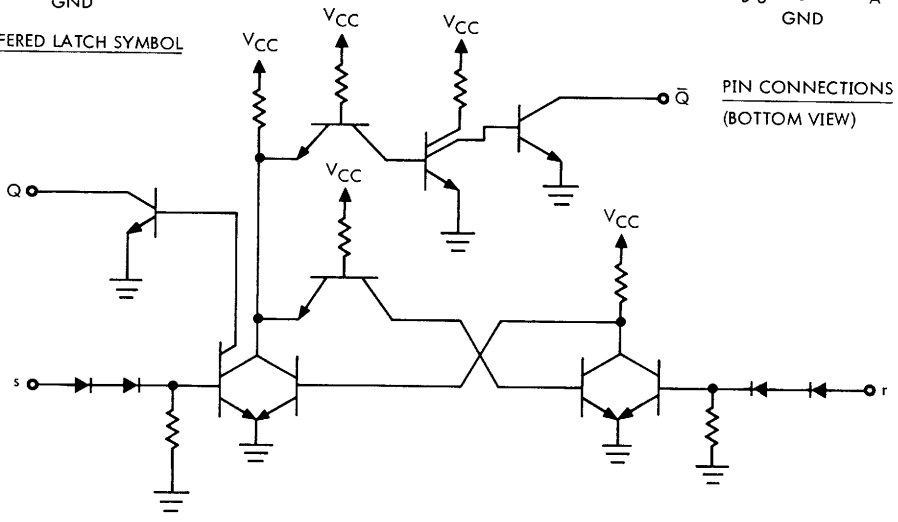
Functional Waveforms



BUFFERED LATCH SYMBOL



PIN CONNECTIONS
(BOTTOM VIEW)



SDS 309 Buffered Latch Schematic

This type of logic is commonly referred to as set-override-reset logic. If the set and reset inputs are true at the same time, the output will follow the set input.

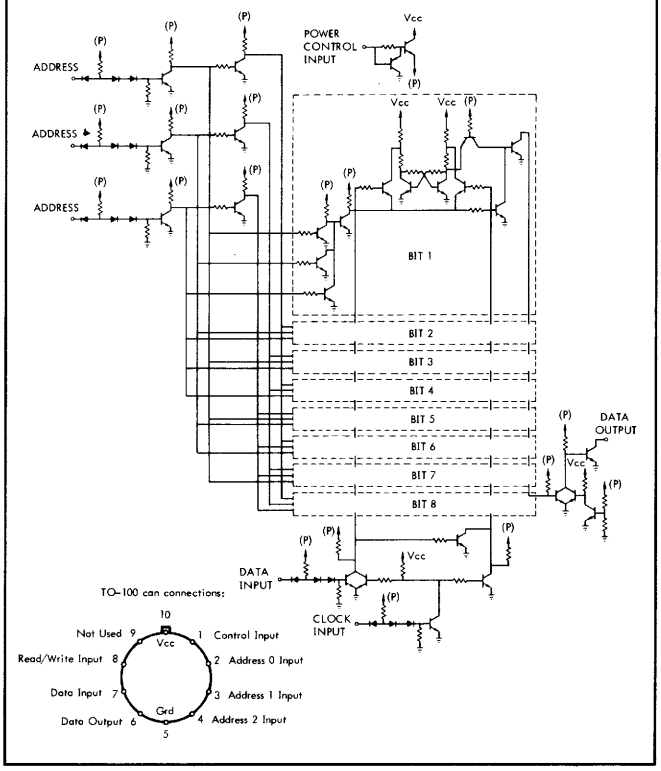
Fast-access Memory Element

The FT40 module uses an integrated storage element which can store eight bits on one integrated circuit. This proprietary IC contains 178 components on a single IC chip. Sixteen ICs plus other logic circuits are mounted on one module to provide addressable, clocked flip-flop storage for 128 bits. The IC schematic is given in the diagram at right. Refer to the FT40 description and module data sheet for additional detail.

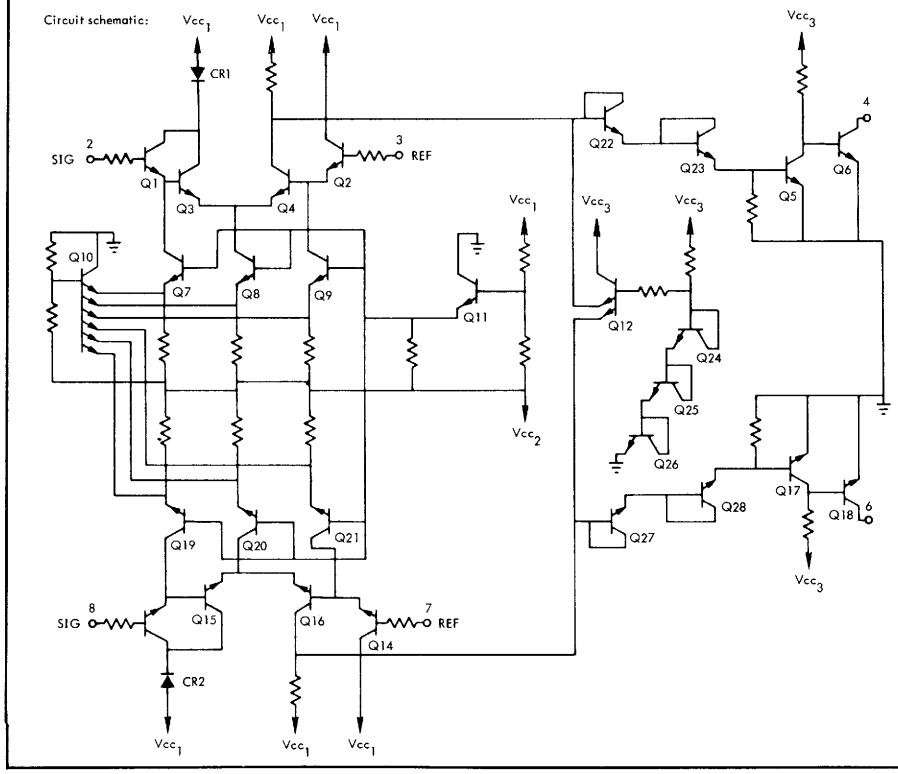
Other Circuits

The supporting circuits such as clock oscillators, one-shots, cable drivers, etc. use a combination of integrated and discrete-component transistor circuits, as is generally the practice where volume of usage or the need for linear amplifiers makes an all-IC approach too costly at full performance. One function that does lend itself easily to integration, however, is the cable receiver circuit, (SDS 308 Discriminator) which is shown below. Circuit schematics of other circuits are given in the module data sheets.

SDS 304 Memory Microcircuit



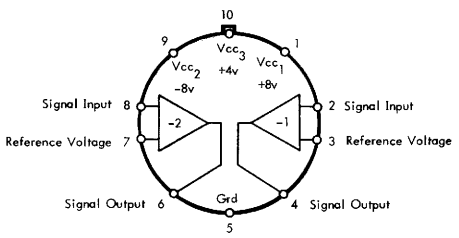
SDS 308 Discriminator Microcircuit



IC Specifications:

Housing:	Two circuits per TO-5 can
Turn-on delay:	40 nsec. max. (50% points)
Turn-off delay:	40 nsec. max. (50% points)
Typical operation:	25 nanoseconds
Output:	Same characteristics as SDS 306 buffer

TO-5 can connections:



II. DESCRIPTIONS OF MODULES

SUMMARY OF MODULE AND ACCESSORY TYPES

Modules are classified as logic element modules, storage element modules, and supporting circuit modules. The logic element modules contain AND, OR, NAND, and NOR gates with non-inverting or inverting amplifiers. The storage element modules contain flip-flops that are used for storage, counting, and shifting. These two broad classes of modules usually form the bulk of a system. Most supporting circuit modules are used to communicate with other equipments or with display devices. Supporting modules include cable driver and receiver modules; interface drivers and receivers to communicate with logic at levels other than 0v and +4v; Schmitt Trigger level detectors for accepting input of arbitrary waveshape; one-shots for precise control of delay; and lamp drivers, relay drivers, and D/A converters for driving display, recording, and mechanical control devices. Also included among supporting modules are the clock oscillators, which furnish the system time reference.

Table 1. LOGIC ELEMENTS PER MODULE

	OUTPUT NOT INVERTED				OUTPUT INVERTED			
Model No.	With Single Input	With AND Inputs	With OR Inputs	With AND/OR Inputs	With Single Input	With AND Inputs (NAND)	With OR Inputs (NOR)	With AND/OR Inputs (AND/NOR)
BT10	-	-	-	8	-	-	-	-
BT11	-	12	-	-	-	-	-	-
BT12	-	2[a]	-	-	-	-	-	-
BT13	-	18[b]	-	-	-	-	-	-
BT18	-	10	-	-	-	-	-	-
BT27	-	-	12	-	-	-	-	-
BT31	2	14	-	-	-	-	-	-
BT33	-	-	-	12[i]	-	-	-	-
FT26	-	-	8[c]	-	-	-	-	-
FT27	-	-	12[c]	-	-	-	-	-
IT10	-	-	-	-	-	-	-	8
IT11	-	-	-	-	-	12	-	-
IT13	-	-	-	-	-	18[b]	-	-
IT14	-	-	-	-	-	-	-	8[d]
IT18	-	-	-	-	-	10	-	-
IT27	-	-	-	-	-	-	12	-
IT31	-	-	-	-	2	14	-	-
LT10	-	4	2	2	3	1	-	-
LT11	-	-	-	4	-	-	-	4
LT26	-	-	-	-	-	-	-	2[e]
LT66	-	2[f]	-	1[g]	-	-	-	-
LT67	-	-	-	h	-	-	-	h

[a] [b] Arranged as 2 separate binary-to-octal decoders
[c] 16 elements in matrix form, 2 independent
[d] With latch inputs grounded
[e] Eight 4-input AND/NORs in 4 x 8 matrix
[f] Two 4-bit switch comparators
[g] Two 12-input AND Gates
[h] One 12-bit comparator
Four full-adders; two bits and carry in, sum and carry out
[i] Arranged as dual-input 12-bit multiplexer

Accessory modules include cable plug modules, breadboard modules, and an extender module. Other accessories include power supplies, cabinets, mounting cases, cables and connectors, wire, and wiring tools. Accessories are described in Section III.

LOGIC ELEMENT MODULES

These modules carry the prefix B, I, or L. Some F prefix modules, the buffered latches, also operate as logic element modules when the latch control inputs are grounded. Table 1, below, lists the modules and shows the assignment of logic functions to modules.

The AND/OR structures may be very simply converted to pure ANDs or ORs by wiring AND inputs True (leaving open) or wiring OR inputs False (grounding). Thus the BT10, IT10, LT10, and LT11 modules can also furnish pure ORs or NORs, if the AND functions are bypassed.

STORAGE ELEMENT MODULES

T Series includes a number of dense and powerful modules which use the high speed, fully gated flip-flops. In addition four latch modules provide low cost storage. A high speed memory module, the FT40, can furnish storage for 128 bits.

SUPPORTING CIRCUIT MODULES

Two types of high density cable driver and receiver modules are offered. AT10, AT11, AT12, AT52 and AT53 are intended for equipment using T Series modules at both ends of the cable. AT47 and AT48 use 0v/+8v logic levels on outputs and inputs respectively, and are designed to interface through cables with other lines of modules such as the SDS discrete-component C, H, and L Series.

TABLE 2. STORAGE ELEMENTS PER MODULE

Model No.	Description	No. F. F. or Latches
FT10	Basic flip-flops with gated set and gated clock inputs	6
FT11	Flip-flops with gating for counter modes	4
FT12	Basic flip-flops with some gated set inputs	8
FT19	Multifunction counter-register	8
FT20	Two 8-bit buffered latch storage registers with fast/slow strobe option	16
FT26	Buffered latch multiplexing matrix with 4-bit AND/OR inputs	8
FT27	Buffered latch multiplexing matrix with 2-bit AND/OR inputs	12
FT40	128-bit IC Memory	128
FT43	Standard flip-flops with individual, strobed, mark and erase inputs	6
FT56	Clocked flip-flops, with common clock line	12
FT57	D-c flip-flops (cross-coupled NORs)	10
FT58	Two 10-bit buffered latch storage registers	20

Two types of interface modules are offered. NT10 and NT11 will drive high level positive True logic (0v/+8v). Any T Series gate can receive high level logic up to +10v, thus no special interface receiver is required to work with NT10 or NT11. NT33 and NT18 interface with negative True logic systems having logic levels down to -12v.

The LT50, LT54, and NT19 modules can be used to interface a digital system with a Teletypewriter or other keyboard-printer, as described in application bulletin 64-51-09.

The adjustable AT22 Schmitt Trigger circuit converts any input waveshape to discrete logic level changes of 0v and +4v.

The ST44 Read-only Memory module recognizes one of eight 16-bit patterns and energizes one of eight lines upon recognition.

The OT18 One-shot provides outputs of adjustable pulse-width from 100 nsec to 20 μsec and has provision for adding external capacitance to permit pulsewidth up to 20 milliseconds. The OT14 One-shot provides outputs from 50 μsec. to 2.2 seconds.

The QT14 Lamp Drivers and RT14 Relay Drivers handle up to 200 ma at 28 volts. QT16 decodes 1, 2, 4, 8 inputs and drives either ten lamps or ten relays.

DT12 and DT13 modules drive analog devices having up to ±20 volt input requirements, in a variety of operating modes. The DT24 provides 9-bit and sign D-to-A conversion at 0.1% accuracy. The WT49 Analog Power Regulator supplies precision + or - 35 volts to sixteen DT24 modules.

The KT10 module provides four SPDT mercury-wetted relays with individual 2-input NAND drivers. The ST14 module provides fifteen SPDT toggle switches on a card.

The HT58 and HT72 are versatile Operational Amplifier modules. The HT72 and AT69 provide sensitive differential receiving capability.

CT16 and CT10 crystal (or LC) controlled clock oscillators provide clock signals in two ranges: 1.8Kc to 2Mc, and 1Mc to 10 Mc, respectively. AT23 and AT24 clock drivers are used when large numbers of clock inputs are driven from the same source.

SPECIFICATIONS

Maximum operating frequency, circuit delays, fan-out, input loads, logic levels, and noise rejection are as described in General Specifications, p. 1, unless otherwise noted in the individual module descriptions.

Module Current Requirements

The maximum current and maximum dissipation listed for each module is for the case where all circuits are in the state which draws maximum current. The inverter and buffer circuits use maximum current when the output is logic 0.

The average current specification given is the current used when the amplifier is on half the time and off half the time. In a system of any complexity the average current instead of the maximum current should be used to determine total power requirements. This gives a more accurate indication of the actual current required.

Only one current specification is given for IC flip-flops because one half of the flip-flop always conducts. Current requirements are therefore independent of output state.

Module Dissipation Ratings

The dissipation figure shown for a module is a worst-case calculation derived from the voltage-current product plus an allowance for IC or transistor dissipation due to load current supplied to other modules. This figure may be used to calculate maximum cooling requirements, but normally will not represent the power required by the module. If average current figures are used, dissipation will also be substantially lower than the dissipation values given.

SUMMARY OF LOADING AND WIRING RULES

LOADING RULES

1. Any 0v/+4v logic output may drive any 0v/+4v logic input.

2. Unless otherwise noted, every gate on a logic line places 1 unit load (3.8 ma) on the driver. Add all gates on a line for total load.

3. Each logic line terminator (220 ohms, on XT10) absorbs 5 unit loads. Maximum is 2 per line, 1 per branch.

4. Every T Series buffer, inverter, or flip-flop output drives 14 unit loads unless otherwise noted. Fan-outs of other circuits are as noted on individual specifications.

5. Buffer, inverter, and flip-flop outputs may be paralleled to form logic functions (see p. 13). Each one paralleled to the first decreases fan-out by 2 loads.

WIRING RULES

General

1. Use No. 28 AWG copper/irradiated KEL-F wire, point-to-point. Push close to ground plane. Refer to Application Bulletin 64-51-07 for a description of wiring techniques.

2. Lay out connections for shortest total wire length. Two branches per line is maximum. Two connections per pin is maximum for both electrical and mechanical reasons.

3. Ground unused flip-flop set inputs (wire False) to avoid set-1 permanently overriding reset. Ground unused flip-flop dc inputs. Ground unused OR inputs. Leave open (True) unused AND inputs.

4. Power pins are: +4v, pin 49; +8v, pin 51; -8v, pin 50. Ground pins are: 0, 16, 32, 48. The +4v, +8v, and ground wiring is built into back panel plane. The -8v must be wired separately to pin 50 when required.

Simplified Rules For Safe Operation Below 2Mhz

Because of relatively long settling time (>500 nsec) T Series logic wiring for use with clock rate under 2 Mhz is simple. Observe these rules:

1. Maximum wire length is 60 inches per branch (max. 2 branches per line).

2. Three stages of series buffers/inverters between flip-flops is maximum unless sum of delays is calculated to be under 500 nsec total.

3. With 3 stages use terminator on at least 1 line if total length of any line reaches 60 inches. With 1 or 2 stages no terminators are required.

Operation Above 2 Mhz Clock Rate

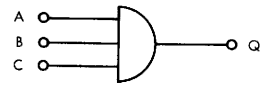
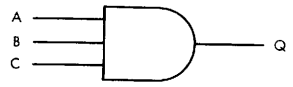
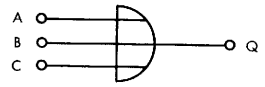
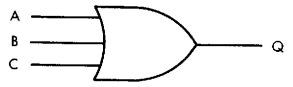
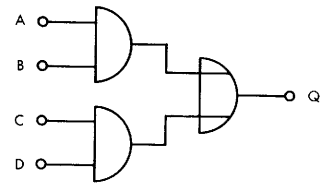
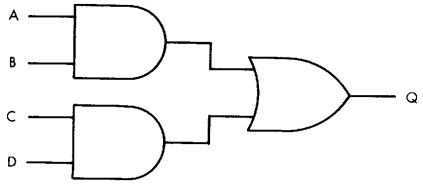
As clock rate is increased less delay can be tolerated in the wiring since active circuit delays are fixed. Line terminators decrease delay on the 0 to 1 transition by decreasing line capacitance charge time. At clock frequencies over 2 Mhz wiring rules are more stringent than those given above, and delays may have to be calculated. Refer to Application Bulletin 64-51-04 for a technical discussion of delay problems and for additional data on wiring delays.

In general, lines under 18 inches need not be terminated but lines over 60 inches must be terminated. Between these boundaries termination is optional and depends on both propagation speeds desired and the magnitude and timing of reflections.

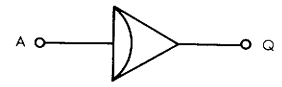
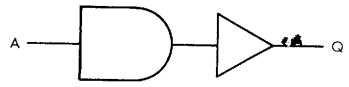
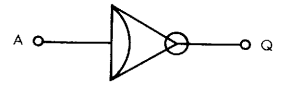
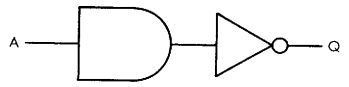
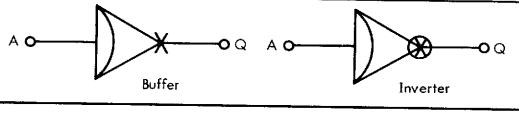
LOGIC SYMBOLS

The SDS logic symbols shown below are used throughout this catalog.
MIL-STD-806B logic symbols are shown beside the SDS symbols for comparison.

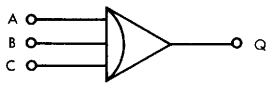
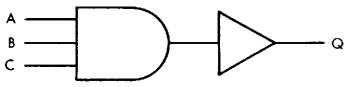
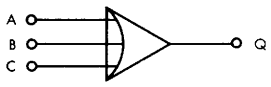
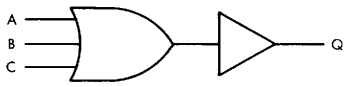
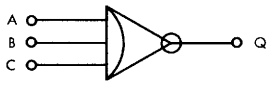
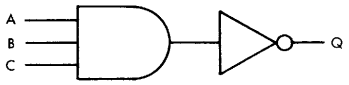
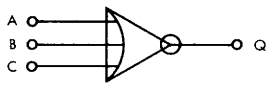
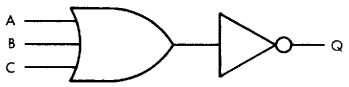
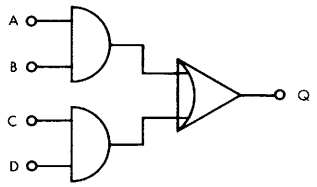
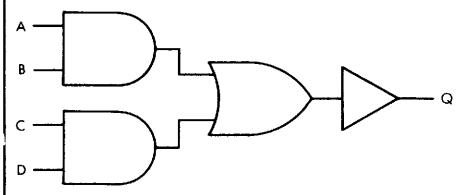
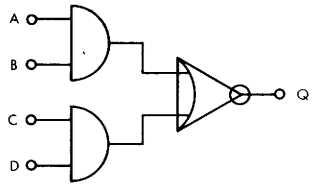
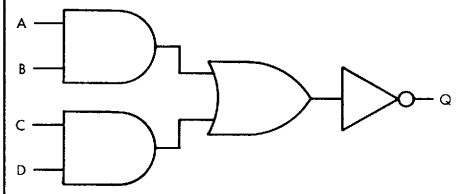
GATES WITHOUT LOGIC AMPLIFIERS

	SDS SYMBOLS		MIL-STD-806B EQUIVALENT
AND Gate		Q=A·B·C	
OR Gate		Q=A+B+C	
AND/OR Gate		Q=A·B+C·D	

LOGIC AMPLIFIERS

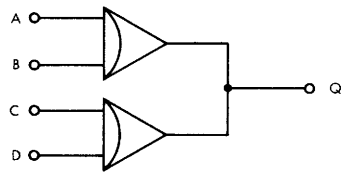
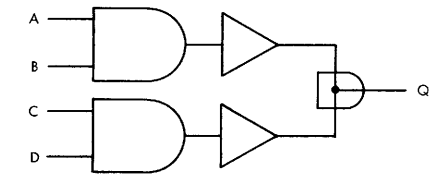
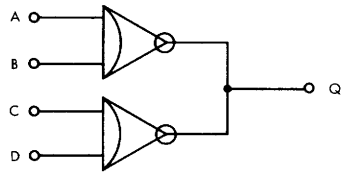
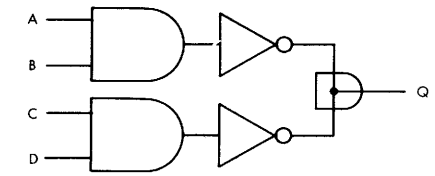
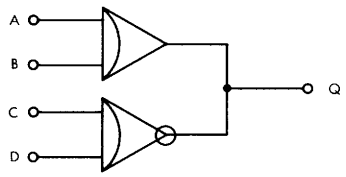
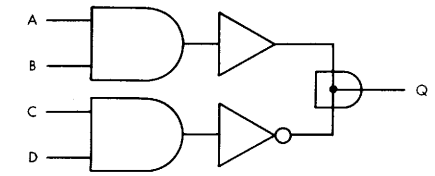
	SDS SYMBOLS		MIL-STD-806B EQUIVALENT
Buffer		Q=A	
Inverter		$\bar{Q} = A$ or $Q = \bar{A}$	
Without pull-up resistor on the module			Pull-up resistor is connected externally. Add note to symbols shown above.

GATES COMBINED WITH LOGIC AMPLIFIERS

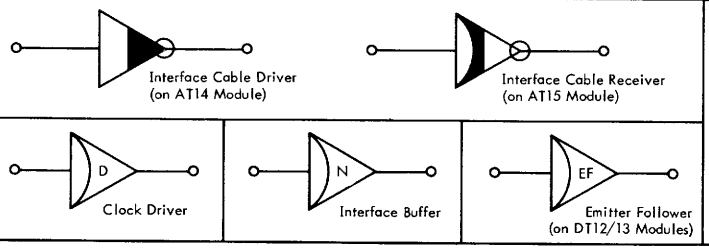
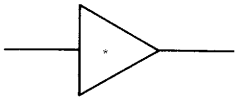
	SDS SYMBOLS		MIL-STD-806B EQUIVALENT
Buffered AND Gate (BAND)		$Q=A \cdot B \cdot C$	
Buffered OR Gate		$Q=A+B+C$	
NAND Gate		$\overline{Q}=A \cdot B \cdot C$, or $Q=\overline{A} \cdot \overline{B} \cdot \overline{C}$ or $Q=\overline{A}+\overline{B}+\overline{C}$	
NOR Gate		$\overline{Q}=A+B+C$ or $Q=\overline{A+B+C}$ or $Q=\overline{A} \cdot \overline{B} \cdot \overline{C}$	
Buffered AND/OR Gate		$Q=AB+CD$	
Inverted AND/OR Gate (AND/NOR)		$\overline{Q}=AB+CD$ or $Q=\overline{AB+CD}$ or $Q=(\overline{A}+\overline{B})(\overline{C}+\overline{D})$	

LOGIC FUNCTIONS FORMED AT OUTPUTS

A T Series feature is the logic function created when two or more amplifier or flip-flop outputs are tied directly together.
The rule is that any element having a false output will cause all outputs connected together to be false.

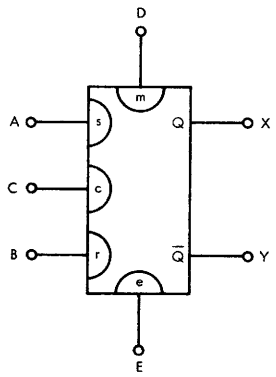
SDS SYMBOLS		MIL-STD-806B EQUIVALENT
	$Q=A \cdot B \cdot C \cdot D$ or $\overline{Q}=\overline{A}+\overline{B}+\overline{C}+\overline{D}$	
	$Q=(\overline{AB})(\overline{CD})$, or $Q=(\overline{A}+\overline{B})(\overline{C}+\overline{D})$, or $\overline{Q}=AB+CD$	
	$Q=(AB)(\overline{CD})$ or $Q=AB(\overline{C}+\overline{D})$	

OTHER AMPLIFIERS

SDS SYMBOLS	MIL-STD-806B EQUIVALENT
	 *Letter is placed inside Symbol to denote function

SDS IC FLIP-FLOP

SDS SYMBOLS	MIL-STD-806B EQUIVALENT



Signal Relationships:

$X = \overline{Y} = D + AC$

(C is falling edge of clock pulse)

$Y = \overline{X} = E + BC\overline{A}$

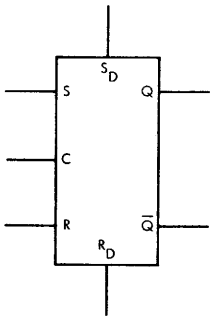
Terminal Designations:

- m = "mark" input (unclocked set input)
- e = "erase" input (unclocked reset input)
- s = set input (must be clocked)
- r = reset input (must be clocked)
- c = clock input (falling edge of clock is used)
- Q = set output $\overline{Q}$ = reset output

TRUTH TABLE

Period n		n + 1
s	r	Q
0	0	Q^n
0	1	0
*1	0	1
*1	1	1

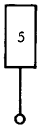
*Note the unique characteristic of the SDS flip-flop: the set input, when True, always causes the Q output to go True (when clocked), regardless of the state of the reset input. Mark and erase inputs, however, always override set and reset inputs. When both mark and erase are True simultaneously both outputs are False until one input goes False; the flip-flop then assumes the state determined by the other input, which was True last. Inputs must be wired False (grounded) when not used. Reset input is wired True (left open) in set-True-overrides-reset applications.



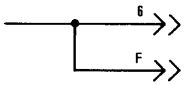
Terminal Designations:

- S_D = set direct (equivalent to SDS m)
- R_D = reset direct (equivalent to SDS e)
- S = set (equivalent to SDS s)
- R = reset (equivalent to SDS r)
- C = clock (equivalent to SDS c)
- Q = 1 output
- $\overline{Q}$ = 0 output

TERMINATORS

SDS SYMBOL	MIL-STD-806B EQUIVALENT
 Line Terminator (absorbs 5 Unit Loads)	

CABLE CONNECTORS



Front edge cable connectors

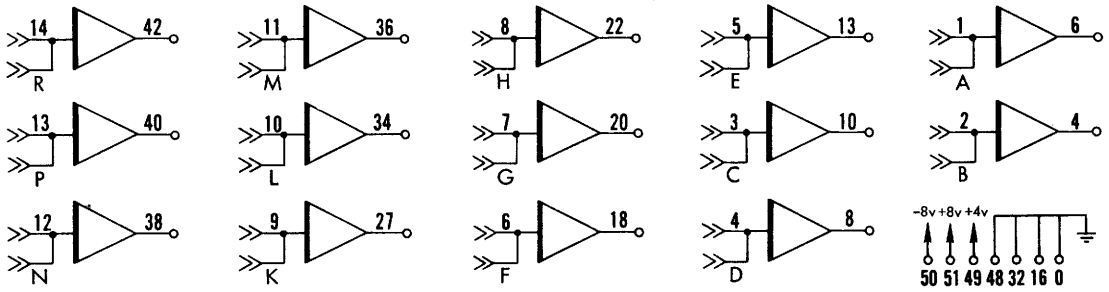
CABLE RECEIVERS

AT10

Model AT10, AT11, and AT12 modules, together with ET cable components, constitute a high-speed logic signal interconnection system for distances up to 200 feet. Logic levels of 0v/+2v are transmitted over 33 ohm coaxial cable. 14-conductor cables are clamped to the front edge of each module with ET11 connectors.

The AT10 module contains 14 identical cable receiver circuits which switch when input exceeds the +0.54v switching value. Output is not inverted. Up to 25 receivers can be connected to the output of 1 cable driver, because input capacitance is very low.

Max. Data Rate:	10Mhz
Circuit Delay:	20 nsec typ., 40 nsec worst case
Input Logic Levels:	0v (Logic 0), +2v (Logic 1)
Switching Threshold:	+0.54v, ±0.1v
Input Range:	-1.5v to +4.4v
Input Current:	50 μa per receiver
Input Capacitance:	8 pf max. per receiver
Output Logic Levels:	0v (Logic 0), +4v (Logic 1)
Output Drive:	14 Unit Loads (53.2 ma) each output
Power Requirements:	+4v, 165 ma av., 256 ma max. +8v, 114 ma av., 153 ma max. -8v, 87 ma av., 117 ma max.
Dissipation:	2.5 watts av., 3.55 watts max.



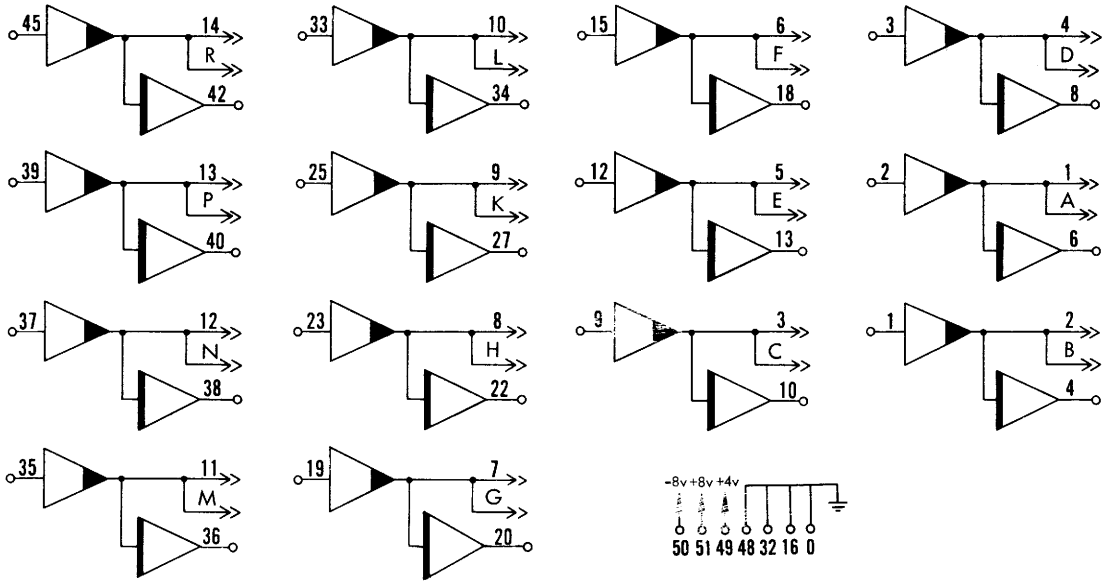
LOGIC DIAGRAM, AT10

CABLE RECEIVERS/DRIVERS

AT11

AT11 contains 14 identical pairs of driver-receivers. Driver outputs are on the same terminals as receiver inputs to reduce space and connectors. Receivers normally use input from drivers at other cable locations, not from the same module. Circuits are identical to AT10 and AT12.

Power Requirements:	+4v, 1.05 amp. av., 2.045 amp. max. +8v, 392 ma. av., 586 ma max. -8v, 87.5 ma. av., 117 ma max.
Dissipation:	15.2 watts max.
Other Specifications:	See AT10 or AT12



LOGIC DIAGRAM, AT11

CABLE DRIVERS

AT12

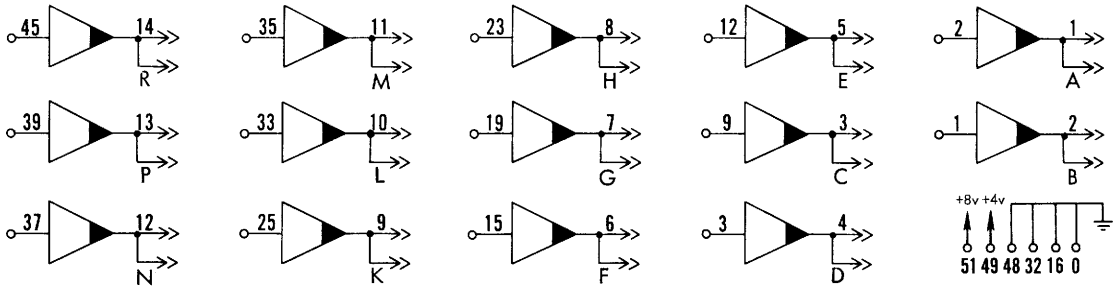
Model AT12 contains 14 identical cable driver circuits which accept standard T Series 0v/+4v logic level input and convert to 0v/+2v logic level output. The AT12 is designed to drive AT10 or AT11 receiver circuits, and has front-edge contacts for ET11 connectors.

Driving capability depends on cable attenuation. Maximum length is 200 feet of 33 ohm coaxial cable. Any number of cable drivers can be placed on one cable but only one driver can be raised True at one time since outputs add.

Input wiring restrictions: back panel wiring cannot exceed 18 inches, and no terminator may be placed on input line.

Max. Operating Freq.:	10 Mhz
Circuit Delay:	5 nsec typ., 10 nsec worst case
Input Logic Levels:	0v (Logic 0), +4v (Logic 1)
Input Current	9 Unit Loads (34 ma)
Output Logic Levels:	0v (Logic 0), +2v (Logic 1)
Output Loading:	16.5 ohms to ground; use two 33 ohm cables or 1 cable and 1 dummy load (ET13)
Power Requirements:	+4v, 805 ma av., 1.78 amps max. +8v, 278 ma av., 433 ma max.
Dissipation:	11.65 watts max.

Refer to Accessories section for cable and connectors.



LOGIC DIAGRAM, AT12

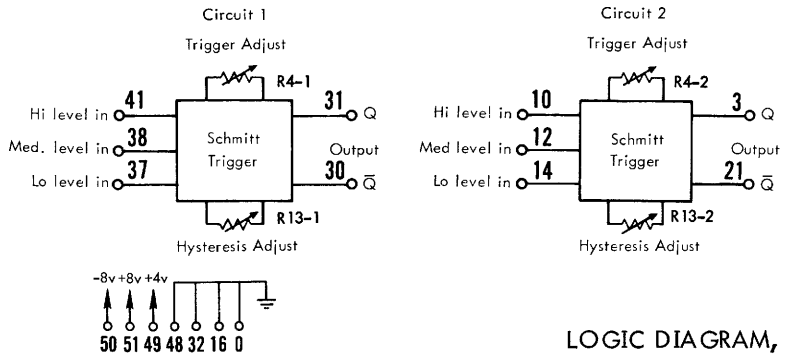
SCHMITT TRIGGERS

AT22

Model AT22 contains two dc-to-10 Mhz Schmitt Trigger circuits. Three input ranges are provided. Each Q output rises to +4v when input exceeds the adjustable trigger level and returns to 0v when input drops below the adjustable hysteresis level, which is always more negative than the trigger level.

The Schmitt Trigger is essential for squaring sine wave or other non-squarewave input. It is also used as a pulse amplifier. A regulator on the module keeps thresholds stable. Outputs are fully buffered.

Circuit Delay:	25 nsec typical
Input Load to Common:	±5v range, 1k ohms ±15v range, 3k ohms ±50v range, 10k ohms
Resolution:	±5v range, ±50 mv ±15v range, ±150 mv ±50v range, ±.5v
Drive Capability:	12 unit loads per output
Power Requirements:	+4v, 10 ma +8v, 35 ma -8v, 50 ma
Dissipation:	0.750 watts max.



LOGIC DIAGRAM, AT22

Table 1. Trigger and Hysteresis Ranges

Trigger (True Threshold)	Hysteresis
±5v	.5v to 1.5v
±15v	1.5v to 4.5v
±50v	4.0v to 17v

AT23

HIGH CURRENT CLOCK DRIVER

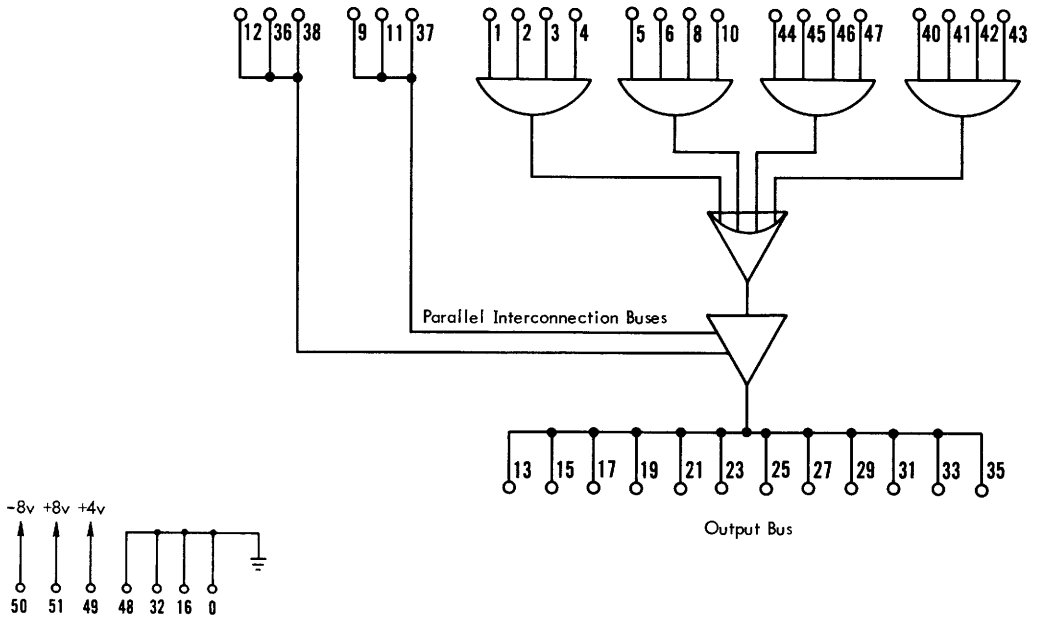
The AT23 is a non-inverting high current driver which can provide clock pulses for twelve 33-ohm clock lines simultaneously. AT23 modules can be paralleled to obtain driver power for additional clock lines. To eliminate skew at the clock source, several internal buses are brought out to pins, for connection to parallel AT23 modules.

Because of high power dissipation, an AT23 should not be mounted in proximity to AT23's or other high dissipation modules. However, AT23 modules connected in parallel should not be separated by more than one module space to minimize skew. The use of ZT23 cable plug modules to inter-leave parallel AT23's is recommended.

To prevent pulse width narrowing at very low duty cycles, connect unused input diodes to +4v through 2.2K ohm resistors.

Turn-on time (typical):	25 nsec
Turn-on time (minimum):	15 nsec
Input-output pulse width difference (pulse narrowing):	6 nsec
Load imposed by each AT23 input:	1 unit load (3.8 ma)
Output drive capability (max.):	1.4 amps (368 unit loads)
Input logic levels:	Logic 1: +4v Logic 0: 0v
Output logic levels:	Logic 1: +4v to +4.7v * Logic 0: 0v
Power requirements:	+4v, 642 ma; +8v, 539 ma; -8v, 150 ma
Dissipation:	8.8 watts max.

*Dependent on load; output can go as high as one diode drop (+.7v) above +4v because of inductors in the output circuit.



LOGIC DIAGRAM, AT23

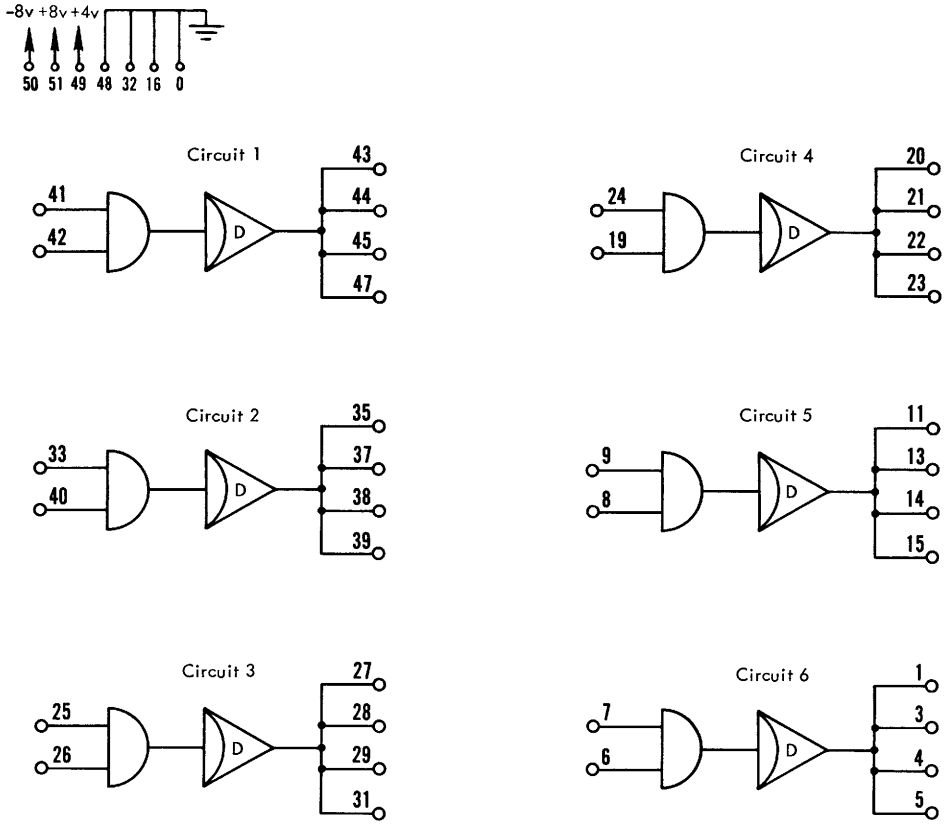
MEDIUM CURRENT CLOCK DRIVERS

AT24

The AT24 contains 6 non-inverting medium current drivers. The AT24 module will drive standard 100-ohm wiring or 33-ohm cable. Each driver circuit can be used to amplify clock pulses or other signals.

AT24 module drivers should not be paralleled when driving clock lines because of the possibility of skew at the clock source. Use the AT23 module for high current requirements. Because of a high power dissipation factor, AT24 modules should not be mounted in proximity to other AT24 modules or other high dissipation modules.

Turn-on time (typical):	25 nsec
Turn-on time (min):	10 nsec
Input-output pulse width difference:	8 nsec
Load imposed by each input term:	1 unit load (3.8 ma)
Output drive capability:	340 ma per driver (88 unit loads)
Input logic levels:	Logic 1: +4v Logic 0: 0v
Output logic levels:	Logic 1: +4v Logic 0: 0v
Power requirements:	+4v, 330 ma; +8v, 544 ma; -8v, 150 ma
Dissipation:	7.9 watts max.



LOGIC DIAGRAM, AT24

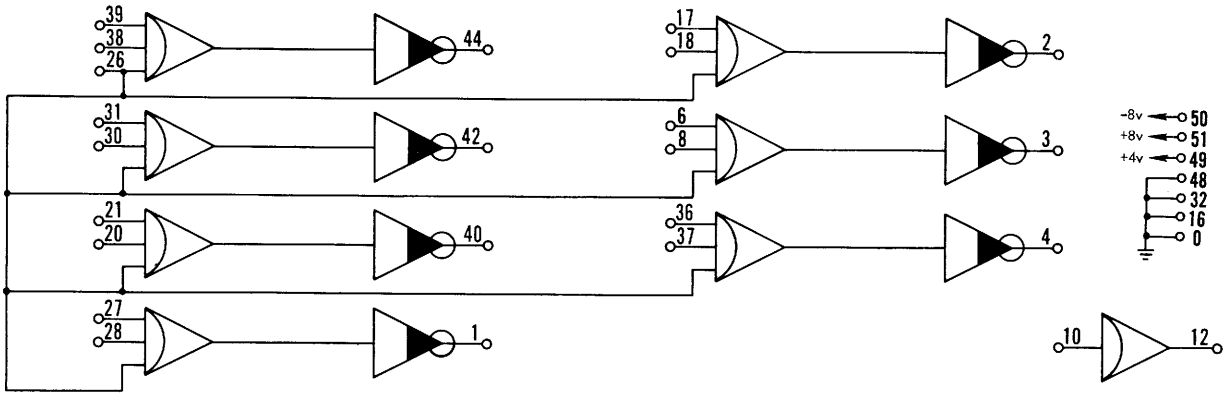
AT47

8-VOLT INTERFACE CABLE DRIVERS

The AT47 module has 7 cable drivers for driving 6 gates each, with 0 and +8v levels, such as are used with SDS C, H, and L series modules. It also contains 1 buffer amplifier. Each cable driver circuit is driven by a T Series 3-input buffered AND with 0v and +4v logic levels; one of the three inputs is common to all gates on the card, for use as a common control line.

The drivers are designed to drive 33 ohm cable. Rise and fall times are about 1 μsec to reach 50% of logic level. If cable length is less than 60 feet the cable may be connected directly to an SDS Model ZX13 cable plug module, which is compatible with the C, H, and L Series modules.

Power Requirements:	+4v: 90 ma av., 119 ma max.
	+8v: 135 ma, -8v: 85 ma (pin 50)
Dissipation:	2.1 watts max.



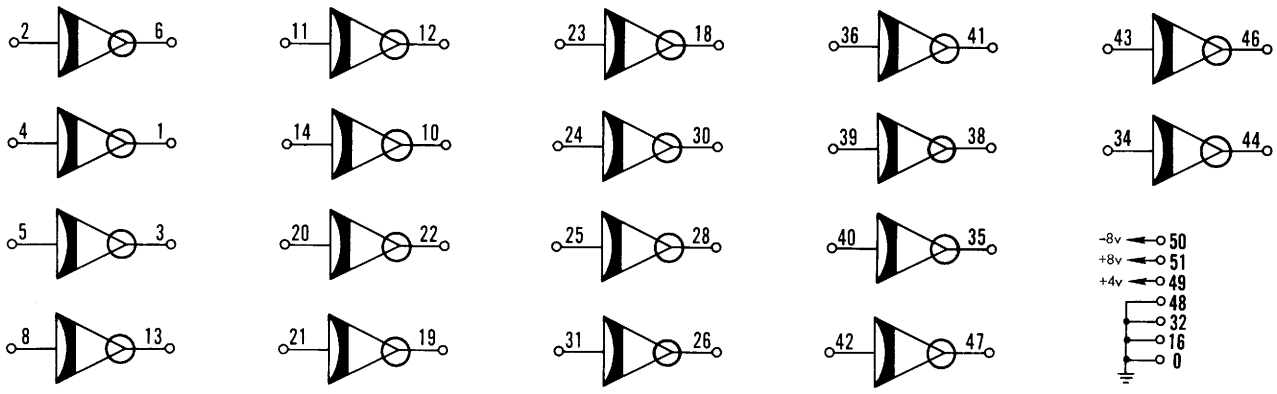
LOGIC DIAGRAM, AT47

AT48

8-VOLT INTERFACE CABLE RECEIVERS

Model AT48 module has 18 cable receiver circuits which will accept logic signals at 0v and +8v levels from a 33 ohm cable input. These circuits may be driven by the Model AT47 cable driver or by 0v and +8v logic signals from SDS B, C, H, K, L, or X Series modules. The output of each receiver is a standard T Series inverter output with 0v and +4v logic levels, capable of driving 14 unit loads.

Switching Time:	$T_{on} \leq 35$ ns; $T_{off} \leq 35$ ns
Power Requirements:	+4v: 145 ma av., 192 ma max.
	-8v: 15 ma (pin 50)
	+8v: 95 ma
Dissipation:	1.5 watts max.



LOGIC DIAGRAM, AT48

TWISTED-PAIR LONG LINE DRIVERS

AT52

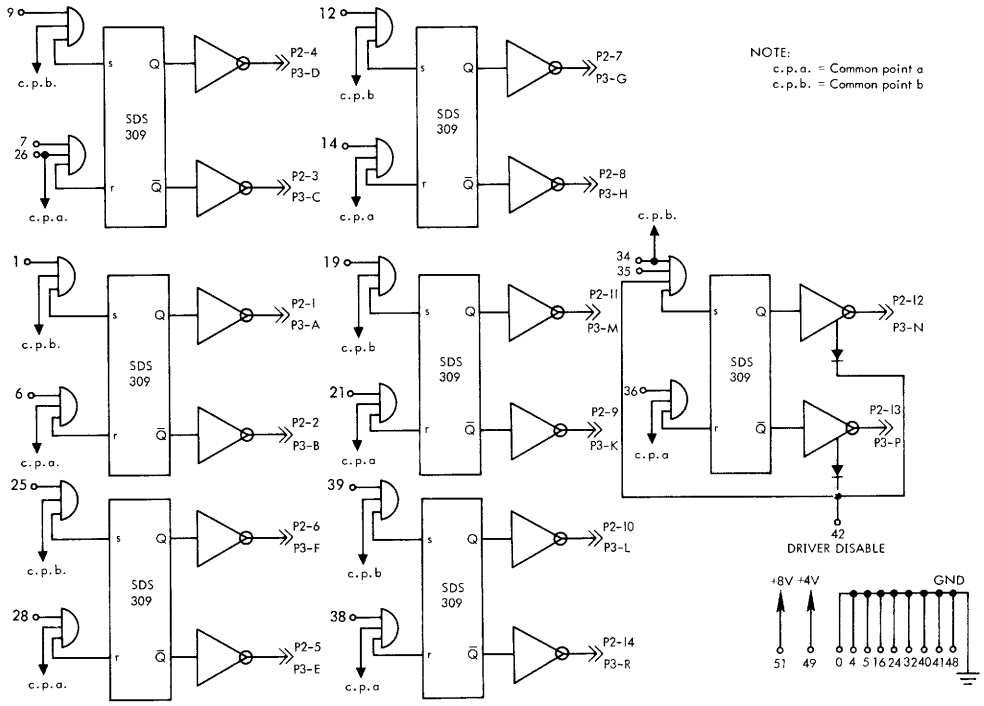
The AT52 Long Line Driver module contains seven SDS 309 buffered latches for signal storage and seven complementary line drivers for signal transmission.

A pair of AT52 Long Line Drivers is designed to work in conjunction with a pair of AT53 Long Line Receivers and ET32-XXXX Long Line Cable Assembly to transmit 14 differential digital signals over distances as great as 2000 ft. at data rates as high as 500 Khz (1.0 Mhz at 1000 ft.). The system is designed for economy and freedom from crosstalk or injected noise.

One driver has an additional circuit tied to its outputs that allows the outputs of that circuit to be disabled by grounding pin 42 through external relay contacts in the event of power failure at the driver. Under this condition, the complementary driver circuit is disabled with both outputs grounded. This condition can then be detected by the fault detection circuit on the AT53 receiver module to reveal that power has failed at the driver.

Line Driver Circuit Specifications:

Max. Data Rate of Module:	1 Mhz
Circuit Delay of Module:	Between 8 and 60 nanoseconds
Input Logic Signals:	
SDS 309 Gate:	
Logic Zero (0):	0 to 0.5 volt
Logic One (1):	4.0 ± 0.4 volts
Driver Disable Pin (42)	
Logic Zero (0):	Must be a relay closure to ground.
Logic One (1):	Must be an open line or pull-ups to +8 volts or a minimum of 560 ohms to +4 volts.
Input Loading:	
Standard Diode Gate:	One unit load
Driver Disable Pin (42):	17 ma
Common Gate Lines (pins 26 & 34):	Seven unit loads
Output Signal Characteristics:	
Module Fan-Out:	One driver can drive one twisted cable pair connected to one AT53 Cable Receiver circuit.
Output Logic Levels:	
Logic Zero (0):	0.6 to 1.3 volts
Logic One (1):	6.0 volts nominal (steady value)
Allowable Cable Lengths:	
Cable:	SDS 149444 (used in Model ET32-XXXX Long Line Cable Assembly)
Length:	70 to 2000 feet at 0 to 500 Khz 70 to 1000 feet at 0 to 1.0 Mhz
Power Requirements:	+4V, 192 ma nominal, 230 ma max. +8V, 600 ma nominal, 720 ma max.
Dissipation:	6.6 watts max.



LOGIC DIAGRAM, AT52

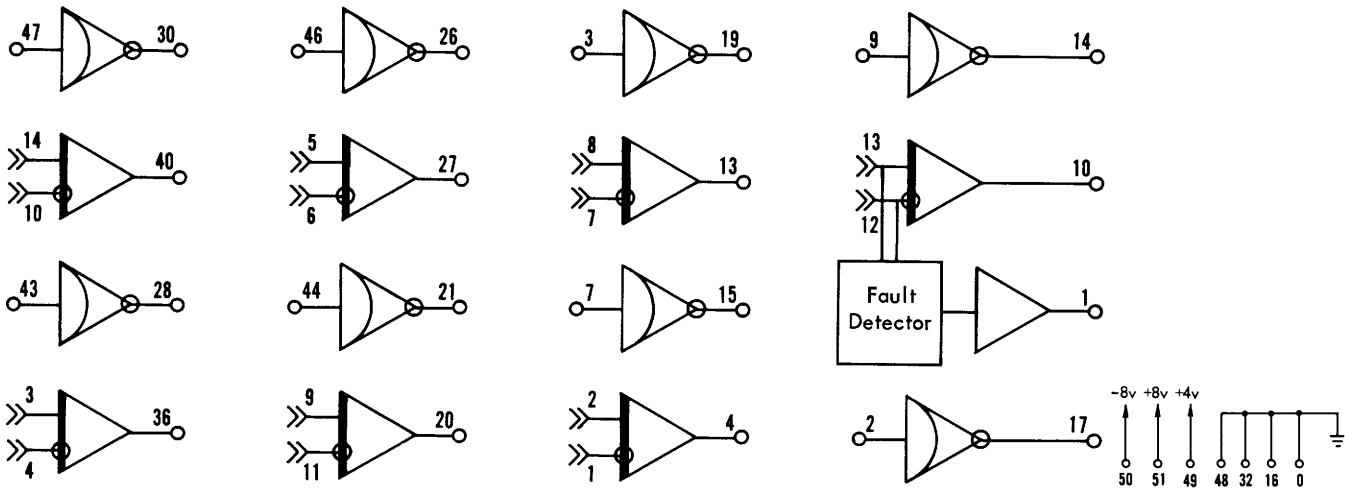
AT53

LONG LINE RECEIVERS

A pair of AT52 modules and a pair of AT53 modules together with one ET32-XXXX Long Line Cable Assembly constitute a balanced twisted pair long line transmission system for 14 digital signals. This system has a bandwidth of 500 Khz at 2000 feet and 1.0 Mhz at 1000 feet. It provides ±7.0V peak common mode rejection.

The AT53 Long Line Receiver module contains seven differential receivers with input termination resistors and eight inverter circuits. One line receiver has an additional circuit tied to its inputs, used to detect the fault condition that occurs when both lines to the receiver input either open or become zero volts. Under this condition, the detection circuit output goes to the logic zero (0) state.

Data Rate:	Dependent on input cable length. 1 Mhz max. (1000 feet of ET32 cable).
Allowable Cable Length:	70 feet to 2000 feet of ET32 cable.
Failure Detector Delay:	Between 1 and 10 μsec.
Input Signal Levels:	Depends on length of cable; guaranteed to operate when driven by AT52 module between length limits listed above. (6V differential at driver end and approximately 2-3V at receiver end).
Common Mode Rejection:	±7V peak
Output Logic Levels:	
Logic One (1):	+4V
Logic Zero (0):	OV
Output Drive of Receiver:	11 unit loads each output except pin 1 which is 1 unit load.
Inverter Specifications:	Standard T Series
Power Requirements: (Entire Module)	+4V, 252 ma av., 315 ma max. +8V, 115 ma -8V, 240 ma
Dissipation:	4.1 watts max.



NOTE:
Termination resistor network at input of each receiver circuit not shown.

LOGIC DIAGRAM, AT53

GENERAL PURPOSE DIFFERENTIAL RECEIVERS

AT69

The AT69 module contains nine independent logic circuits with differential inputs (see connection diagram). When the voltage at the + input becomes at least 1 volt more positive than the voltage at the - input, and remains in that condition for at least 100 nsec, the output goes to logic 1 (high) level. It reaches this level 170 nsec after the input rising edge. When the differential between + and - inputs falls below 1 volt, the output falls 100 nsec later. An open circuit at the inputs also results in an output of logic 0 (low). Either a negative-going or positive-going signal is acceptable, since the circuit is sensitive only to the relative polarity of the input pair.

A differential receiver normally receives digital signals, over shielded cable or twisted-pair lines. A differential receiver has the advantage over a single-ended receiver that it rejects common-mode noise and ground potential differences. Common-mode voltages are those which appear between the two ends of a cable but are common to both of the input leads of the cable. With the AT69, a common mode rejection range of ±volts is provided when +8 volts and -8 volts are used as +V and -V. This rejection range can be increased to ±12 volts with ±V at ±15V.

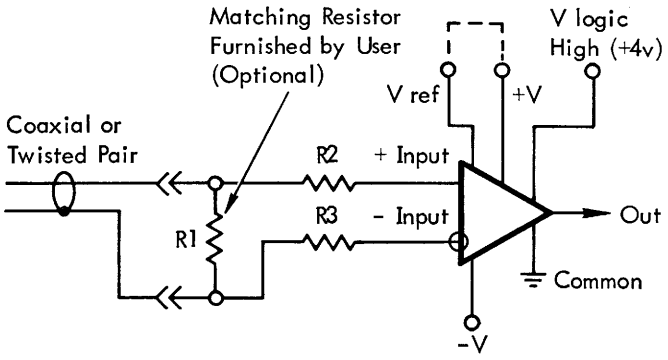
The maximum input data rate is 4 Mhz. A filter network across the input terminals rejects all transients of up to 100 nsec duration, and should be removed when operating above 1 Mhz. This filter furnishes an ac noise rejection which is in addition to the dc noise margin provided by the 1 volt threshold.

The optional resistor R1 (see connection diagram) functions as an impedance matching resistor for the input cable, and is provided by the user to match his particular cable impedance.

The AT69 output high logic level is determined by the supply voltage connected to pin 26, which for T Series use is +4v.

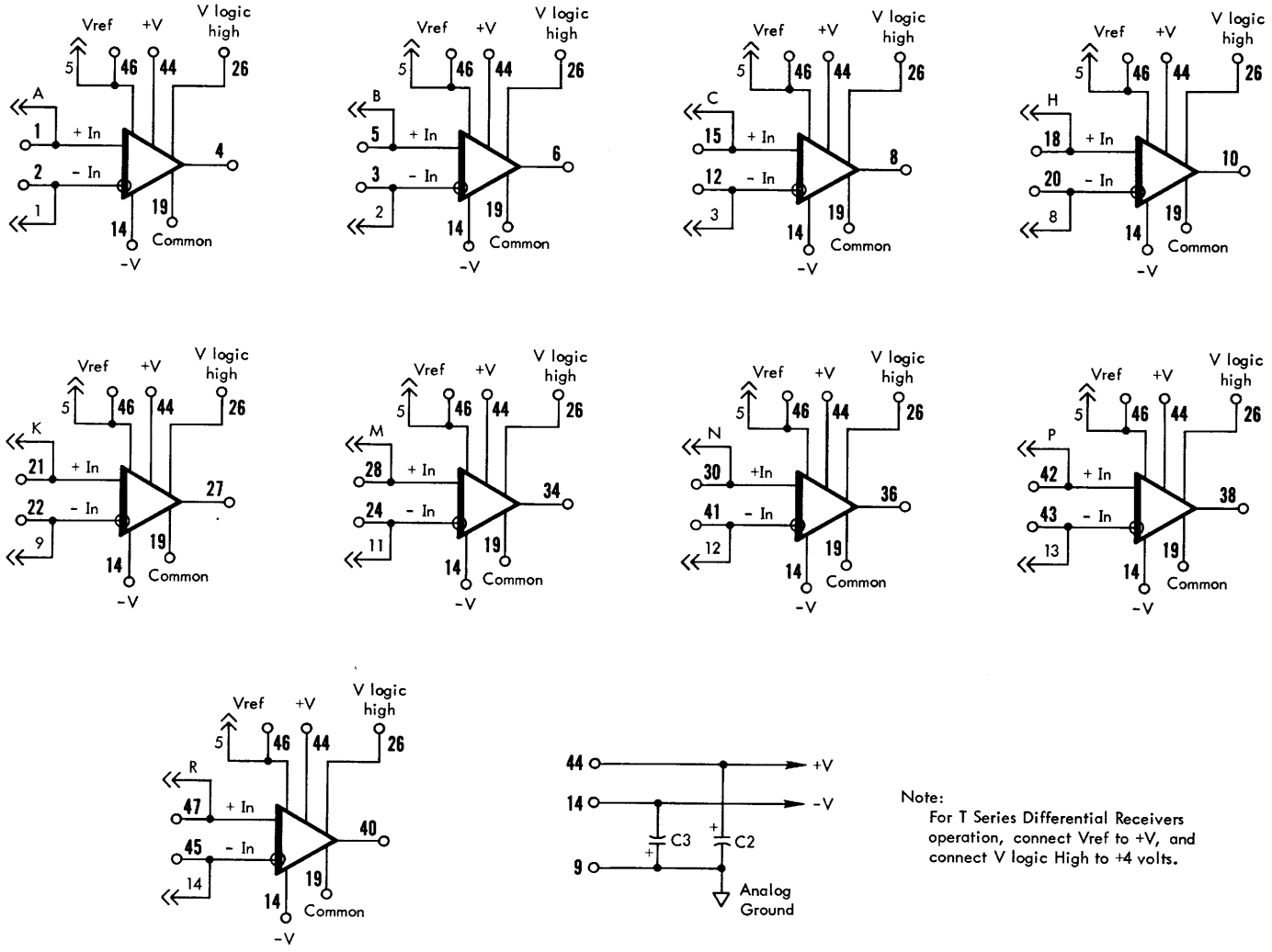
Both input terminals and the Vref terminal are available at front-edge cable connectors (⟶⟫) as well as backpanel connectors (⊸○). The Vref terminal must be connected externally to +V as shown in the connection diagram. The circuit will not operate without the jumper.

The AT69 uses the same basic etched circuit board and most of the same circuit components as the HT73 Comparator Module.



Connection Diagram, One Circuit

Max. Data rate:	4 Mhz
Differential threshold (at + input with respect to - input):	1 volt ±20%
Max. input voltage:	10 volts
Input impedance (without R1):	200K ohms min.
Input pulsewidth (with filter in place):	100 ns min.
Common mode rejection range (with ±8v at +V and -V):	±5 volts
Common mode rejection range (with ±15v at +V and -V):	±12 volts
Fan-out, into T Series:	37 unit loads
Propagation delay, at 25°C:	
To rising edge of output	170 ns typ.
To falling edge of output	100 ns typ.
+4 volt supply (Vcc):	60 ma typ. 68 ma max.
+8 volt supply:	220 ma typ. 270 ma max.
-8 volt supply:	16 ma typ. 25 ma max.
Dissipation, per module:	2.27 watts typ., 3.07 watts max.



Note:
For T Series Differential Receivers operation, connect Vref to +V, and connect V logic High to +4 volts.

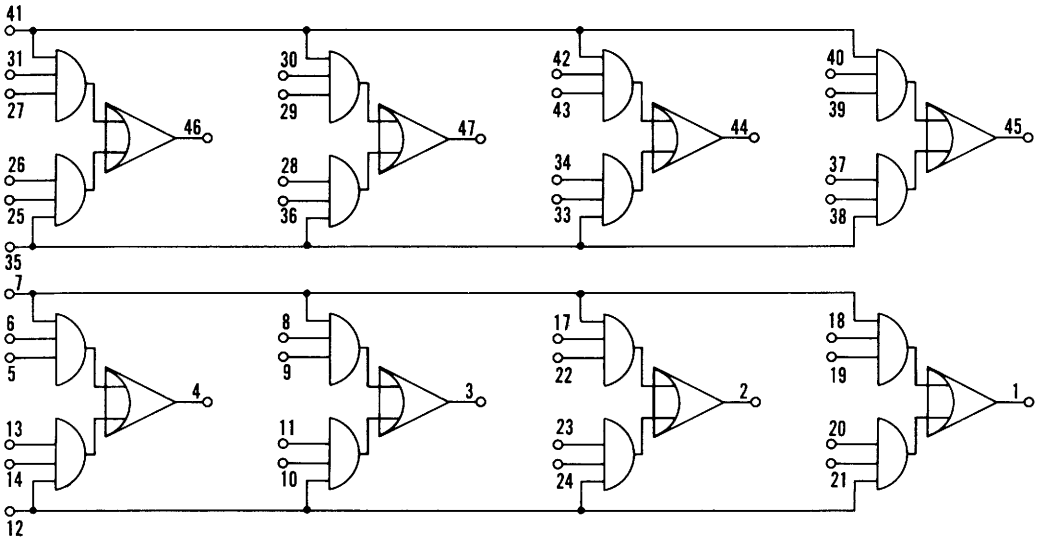
LOGIC DIAGRAM, AT69

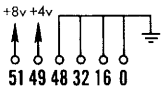
BUFFERED AND/OR GATES

BT10

Eight AND/OR gate structures are on this module. Each circuit consists of two 3-input AND gates, the outputs of which are ORed and amplified. One input on each AND gate is shared with 3 other circuits. The circuits are designed to implement expressions of the type A·B·C+D·E·F. By connecting BT10 circuit outputs together an AND function can be generated, of the type (A·B·C+D·E·F)(G·H·I+J·K·L). The IT10 module has logically equivalent inputs and common connections but its outputs are inverted (refer to IT10 description).

Power Requirements: +4v, 95 ma av., 156 ma max.
+8v, 45 ma av., 57.5 ma max.
Dissipation: 1.2 watts max.





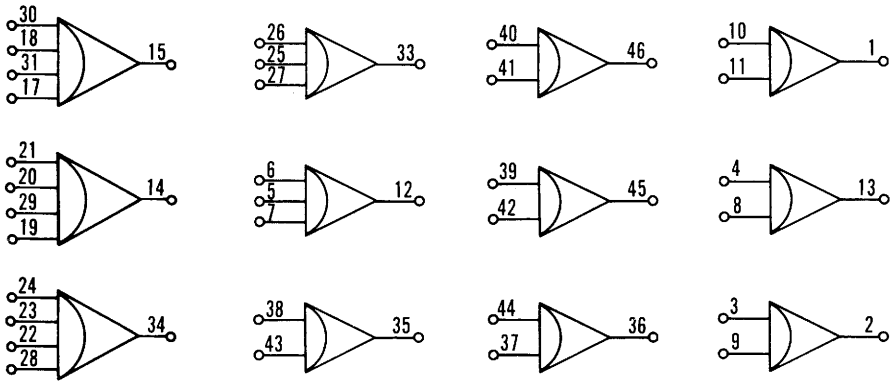
LOGIC DIAGRAM, BT10

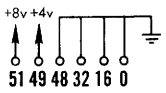
BUFFERED AND GATES

BT11

The BT11 has an assortment of Buffered AND gates for general purpose use. There are two 3-input circuits; three 4-input circuits; and seven 2-input circuits. The AND functions can be expanded by connecting buffer outputs together. The IT11 module has the same configuration of gates but all model IT11 amplifiers are inverters (refer to IT11 description).

Power Requirements: +4v, 142 ma av., 234 ma max.
+8v, 33.6 ma av., 43 ma max.
Dissipation: 1.45 watts max.





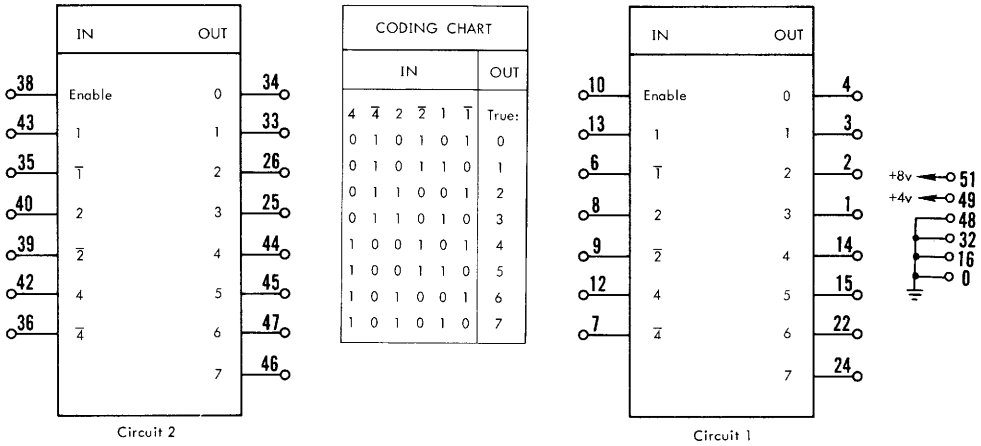
LOGIC DIAGRAM, BT11

BT12

BINARY-TO-OCTAL DECODERS

BT12 has 2 independent binary decoders. Each accepts 3-bit inputs and produces an output on one of 8 pins. In addition, Enable input prevents any outputs from being True when it is False. Enable is used when decoding numbers larger than 3 bits. Using Enable as the fourth input, 2 circuits can decode a 4-bit input so that only 1 out of 16 outputs is True at one time. Each output drives 14 unit loads. Enable input requires 8 unit loads, all others 4 unit loads.

Power Requirements: +4v, 182 ma av., 312 ma max.
+8v, 45 ma av., 57.5 ma max.
Dissipation: 1.88 watts max.



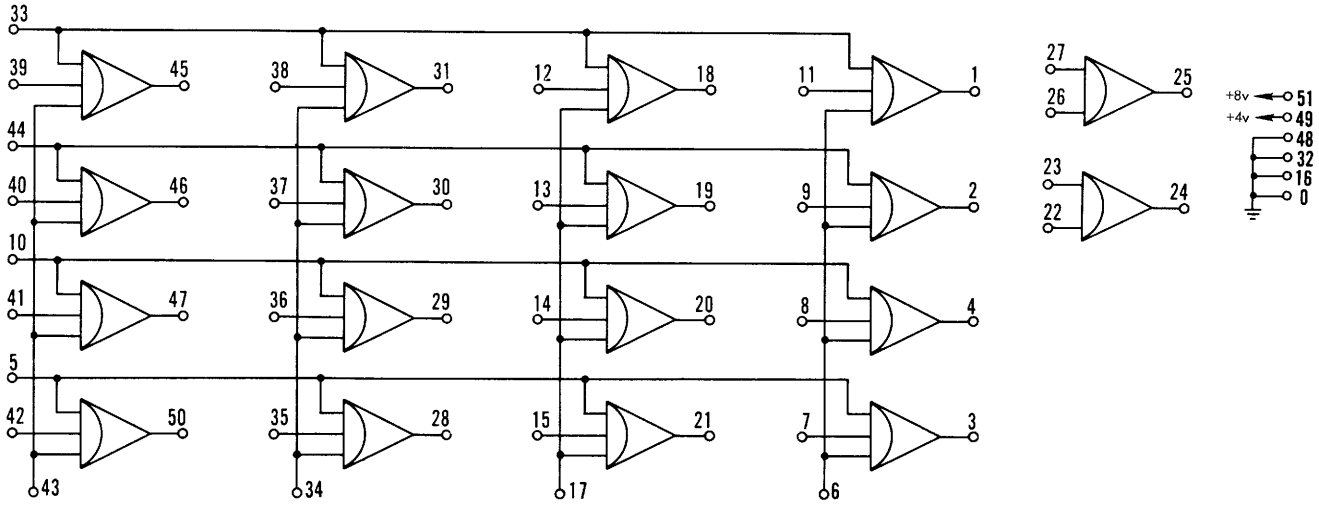
LOGIC DIAGRAM, BT12

BT13

BUFFERED MATRIX

BT13 has a 4 x 4 matrix which can (1) select one of up to 4 groups of 4 bits each, or (2) generate up to 16 discrete outputs from a 4 x 4 matrix input, or (3) provide 18 general purpose amplifiers when all common lines are left open (True). IT13 has the same input logic configuration but outputs are inverted (refer to IT13 description).

Power Requirements: +4v, 230 ma av., 375 ma max.
+8v, 50.4 ma av., 64.6 ma max.
Dissipation: 2.2 watts max.



LOGIC DIAGRAM, BT13

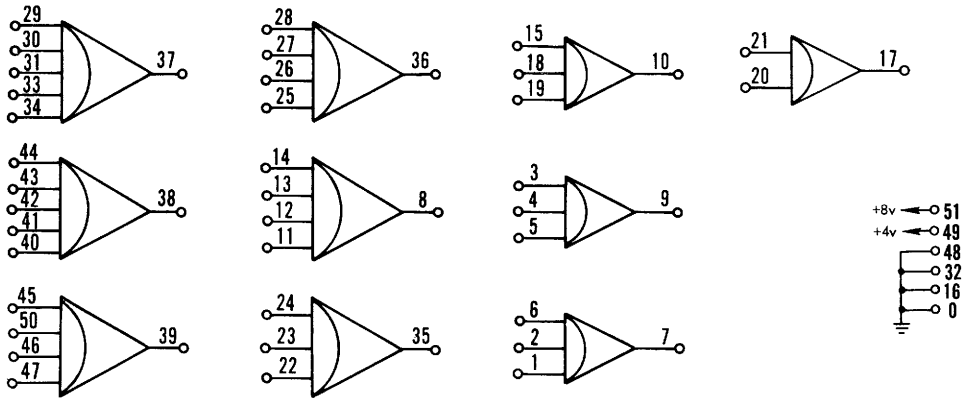
BUFFERED AND GATES

BT18

This module contains ten AND circuits intended for general purpose use. Each circuit can drive 14 loads. Outputs may be paralleled with other circuits; however, each paralleled output decreases the output drive capability by 2 unit loads. The IT18 module has an identical gate configuration but all outputs are inverted (refer to IT18 description).

Power Requirements: +4v, 136 ma av., 219 ma max.
+8v, 28 ma av., 36 ma max.

Dissipation: 1.07 watts max.



LOGIC DIAGRAM, BT18

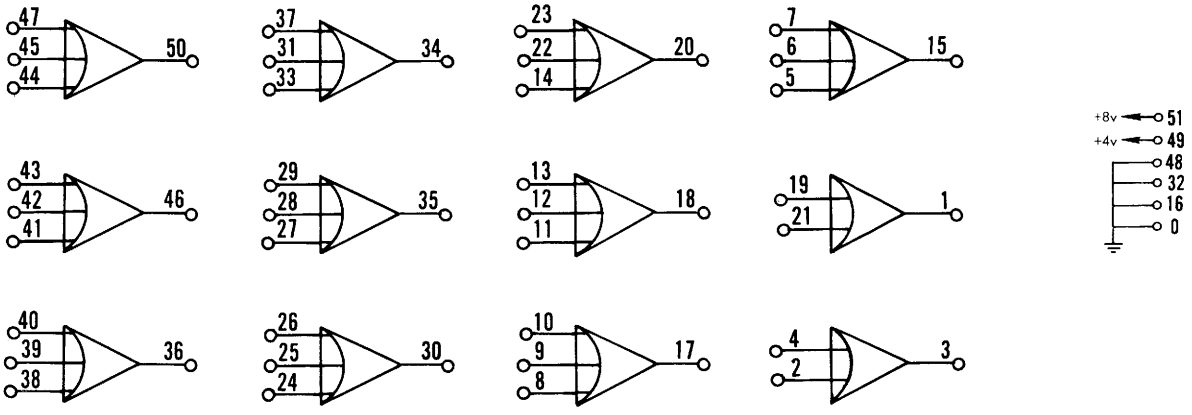
BUFFERED OR GATES

BT27

The BT27 module contains ten 3-input OR gates and two 2-input OR gates intended for general purpose use. Each circuit can drive 14 loads. Various methods are available to expand an OR gate, to form OR-ANDS or by adding a second level of OR gates. The IT27 module has an identical gate configuration but all outputs are inverted (refer to IT27 description).

Power Requirements: +4v, 142 ma av., 234 ma max.
+8v, 95 ma av., 122 ma max.

Dissipation: 2.1 watts max.



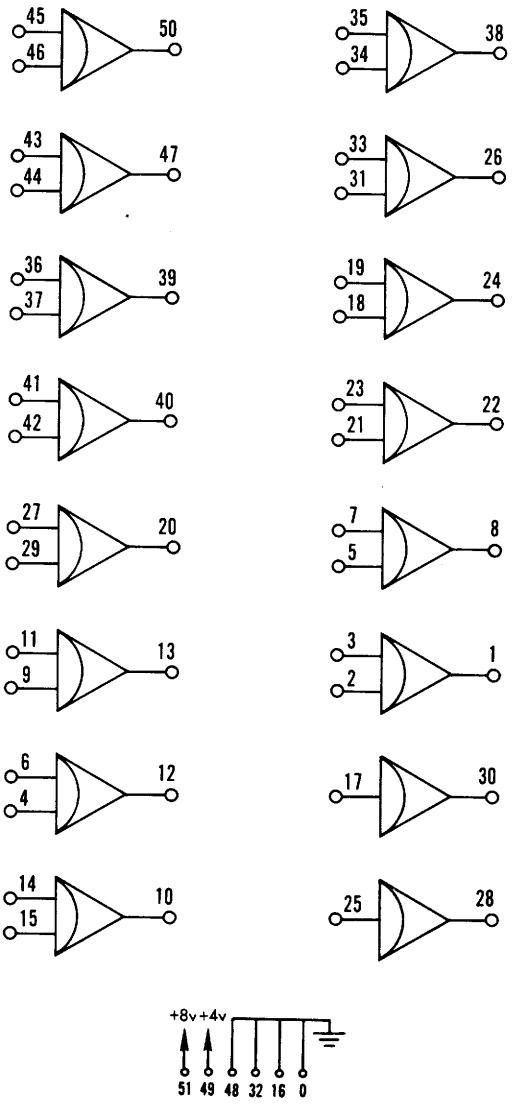
LOGIC DIAGRAM, BT27

BUFFERED AND GATES **BT31**

This module contains fourteen economical 2 - input AND gates and two 1-input buffer amplifiers intended for general purpose use. Each circuit can drive fourteen unit loads. Gates can be expanded by paralleling outputs, with the usual fan-out restrictions. The IT31 module has an identical gate configuration but its outputs are inverted (see IT31).

Power Requirements: +4v, 182 ma av., 312 ma max.
+8v, 45 ma av., 57.5 ma max.

Dissipation: 1.88 watts max.



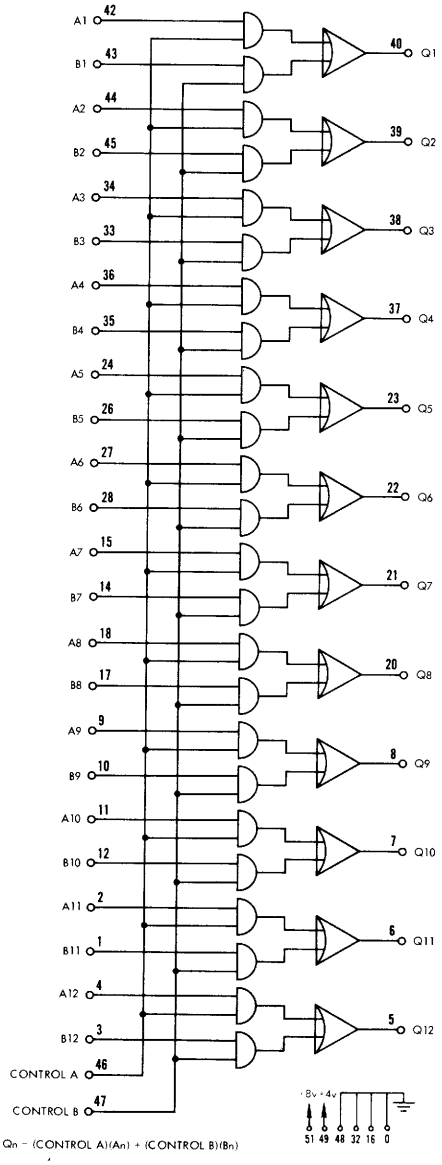
LOGIC DIAGRAM, BT31

DUAL-INPUT 12-BIT MULTIPLEXER **BT33**

The BT33 contains twelve buffered AND-OR gates arranged as a 12-bit multiplexer. It accepts two 12-bit inputs and produces a single 12-bit output, whose state is controlled by the condition of the two control lines. If one control line is True and the other False, output equals the input whose control line is True. If both controls are False, output is all zeros. If both controls are True, each output bit is the OR of the two corresponding input bits.

Power requirements: +4v, 141.5 ma av., 234 ma m
+8v, 67 ma max., 86 ma max.

Dissipation: 1.79 watts max.



LOGIC DIAGRAM, BT33

HIGH FREQUENCY CLOCK OSCILLATOR

CT10

The CT10 contains a 1 Mc to 10 Mc oscillator, a pulse shaper, and a gated clock amplifier (driver). Oscillator is controlled by adjustable LC or optional crystal. External jumpers select range (Table 1). When crystal control is desired specify frequency. When using crystal, first adjust to approximate frequency by LC control with jumper 45-20 in place. Then remove jumper 45-20 and insert crystal. Pulse-width control adjusts duty cycle from 40% to 60%. This adjustment is frequency dependent.

Logic wiring can be used as clock bus. Terminate logic wire clock bus with 220 ohm resistor on XT10 module. Lines should radiate from driver in equal lengths to avoid clock skew.

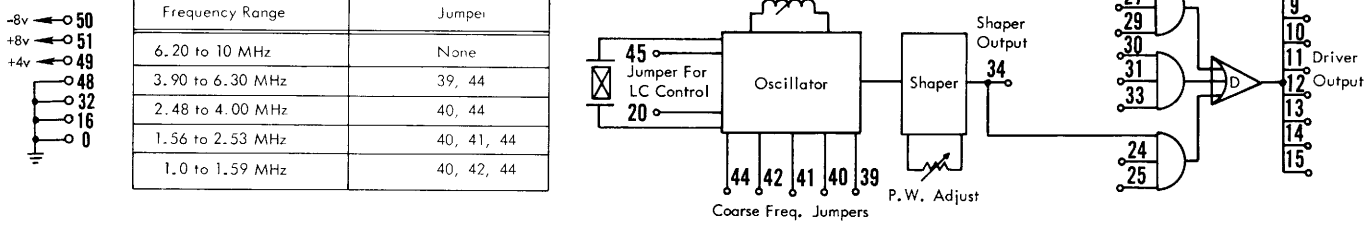
Driver control gate permits frequency division. Ground unused gate inputs.

This module requires two card slots.

Frequency range:	1 Mhz to 10 Mhz
Stability, crystal operation:	2 p.p.m. per °C
Crystal freq. accuracy:	±0.02%
Driver fan-out:	60 unit loads (278 ma)
Shaper fan-out:	7 unit loads (26.6 ma)
Gate inputs:	2 unit loads ea.
Power requirements:	+4v, 40 ma
(at 50% duty cycle)	+8v, 130 ma
	-8v, 60 ma
Dissipation:	1.7 watts max.

TABLE 1. LC CONTROL RANGES

Frequency Range	Jumper
6.20 to 10 MHz	None
3.90 to 6.30 MHz	39, 44
2.48 to 4.00 MHz	40, 44
1.56 to 2.53 MHz	40, 41, 44
1.0 to 1.59 MHz	40, 42, 44



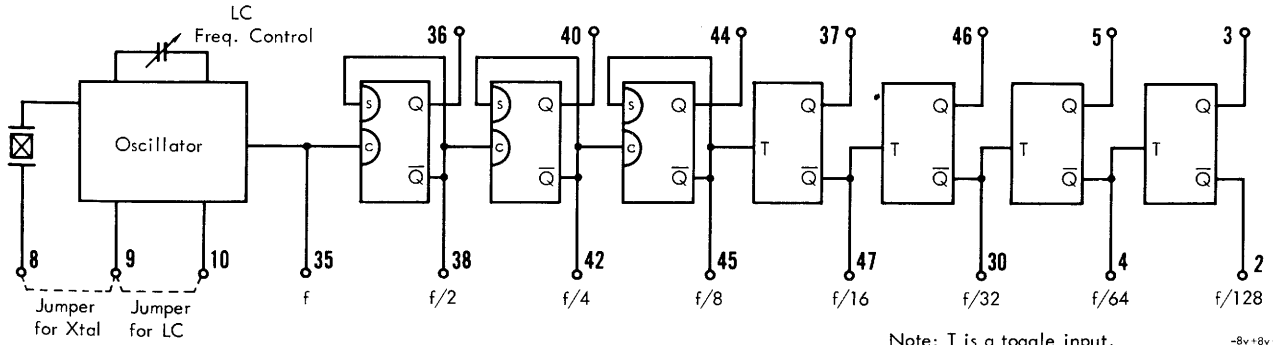
LOGIC DIAGRAM, CT10

MEDIUM FREQUENCY CLOCK OSCILLATOR

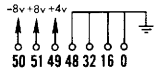
CT16

The CT16 has a 1 Mhz to 2 Mhz oscillator with 50% duty cycle squarewave output, and a seven stage down-counter. Oscillator is controlled by LC or crystal. For higher output drive capability add buffer modules. Clock should be bussed via logic wiring. A 220 ohm terminator must be used (on XT10). Lines should radiate from driver in equal lengths to avoid clock skew. When using more than one frequency take into account the phase shift through the ripple counter.

Frequency range:	7.8 Khz to 2 Mhz
Stability, crystal operation:	2 p.p.m. per °C
Crystal freq. accuracy:	± 0.02%
Fan-out:	Pins 35, 36, 38, 40, 42, 44 45: 13 loads; all others, 10 loads
Power requirements:	+4v, 240 ma
(at 50% duty cycle)	+8v, 85 ma
	-8v, 52 ma
Dissipation:	2.1 watts max.



Note: T is a toggle input.



LOGIC DIAGRAM, CT16

DT12,DT13

4-BIT AND 6-BIT D/A CONVERTERS

Each module has two D/A converters designed for low cost applications where high accuracy is not required. DT12 converters accept 4 bits; DT13 converters accept 6 bits. The DT12-1 and DT13-1 modules also include a reference regulator, and buffer amplifiers, as shown in the diagrams below. The DT12 modules can also be connected (with additional resistors) to accept BCD inputs.

The converters operate with unipolar output. With additional resistors they can also provide bipolar output. The conversion table below, gives output value vs. input code. Note that in the bipolar mode the input codes for negative values must be in 2's complement form if binary, and in 10's complement form if BCD.

An external reference source of maximum +20v on $+E_{ref}$ (plus additional -20v on $-E_{ref}$ for bipolar output) can be used. If the +5v internal reference source is used, one buffer amplifier must be connected between regulator output and converter E_{ref} input. The same amplifier can also supply 14 additional converters, but where isolation between converter units is essential a separate buffer amplifier between regulator output and E_{ref} input should be used for each converter. A buffer can be used on E_{out} when E_{ref} is +5v or less, or in bipolar operation with +5v and -5v reference voltages.

Input-Output Specifications

1. Converter (switches and precision resistor network)
   a. Accuracy: ±1.0% relative to reference voltage
   b. Switch offset: +50 millivolts typical
   c. Output impedance: 5K ohms ±1%
   d. Inputs: standard T Series logic levels, 1 unit load
   e. Output voltage: as given in conversion table
   f. Conversion rate: 400 Khz max.
   g. Settling time (to ±150 mv of f.v.): 2.5 µsec after input signal completes switching. Open output.
2. Buffer amplifier (emitter follower)
   a. Accuracy: ±1.0%
   b. Output range: -1.67v to + 5v
   c. Offset: ±100 millivolts typical
   d. Loading capability: ±10 ma max.
   e. Input impedance: 150K ohms min. at dc
   f. Output impedance: 50 ohms typical
   g. Settling time: 2 µsec. max. to ±50 mv of final value, 1 µsec. max to ±150 mv of final value
3. +5v reference regulator
   Output voltage adjustable to ±0.1%; current: 0.2%

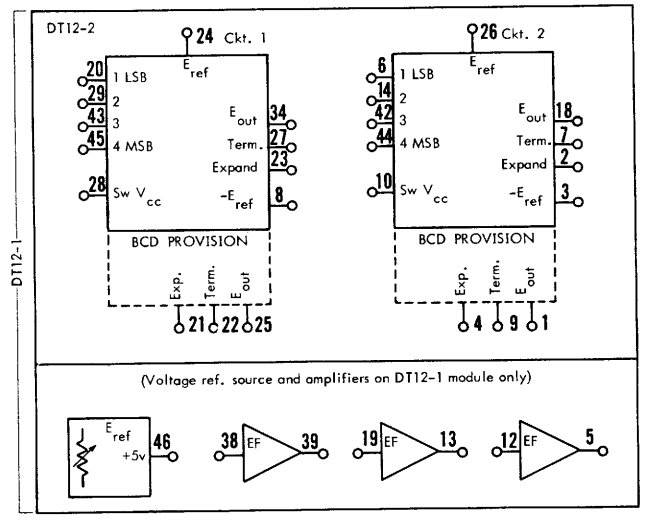
Power Specifications (max.)

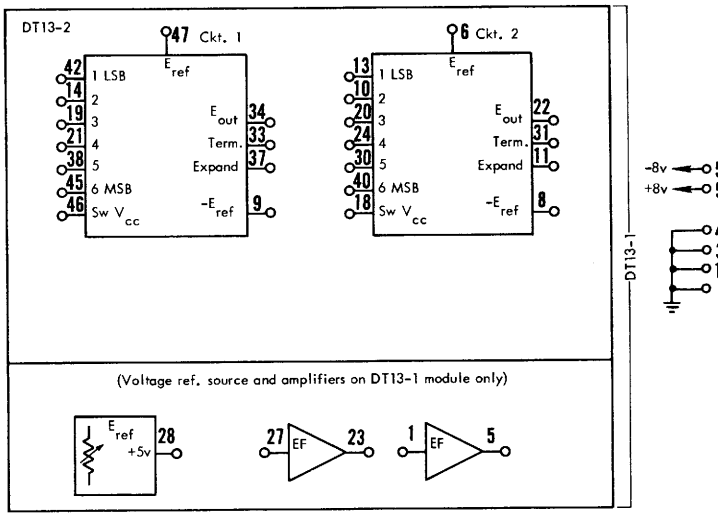
1. Each bit (switch and resistor): +8v, 7.6 ma; -8v, 1 ma (pin 50)
2. Each amplifier: +8v, 50 ma; -8v, 50 ma (pin 50)
3. +5v reference regulator: +8v, 35 ma

CONVERSION TABLE

*n = number of magnitude bits
d = number of decimal digits

INPUTS						Eout, BINARY Operation		Eout, BCD Operation
2^5	2^4	2^3	2^2	2^1	2^0	UNIPOLAR		UNIPOLAR
0	0	0	0	0	0	Full Scale	Eref $(1-1/2^n)$*	0.6 Eref $(1-1/10^d)$*
1	1	1	1	1	0	LSB	Eref/2^n	0.6 Eref/10^d
1	1	1	1	1	1	0	0 volts	0 volts
sign bit	magnitude bits					BIPOLAR (MSB is sign bit)		BIPOLAR (MSB is sign bit)
0	0	0	0	0	0	+Full Scale	1/3 (+Eref)$(1-1/2^n)$	0.2 (+Eref) $(1-1/10^d)$
0	1	1	1	1	0	+LSB	1/3 (+Eref/2^n)	0.2 (+Eref/10^d)
0	1	1	1	1	1	0	0 volts	0 volts
1	0	0	0	0	0	-LSB	1/3 (-Eref/2^n)	0.2 (-Eref/10^d)
1	1	1	1	1	1	-Full Scale	1/3 (-Eref)	0.2 (-Eref)





9-BIT AND SIGN D/A CONVERTER

DT24

The DT24 is a high accuracy 9-bit and sign digital-to-analog converter with ±4 ma or ±10 volts (±20 ma) bipolar output. The module includes a resistive ladder network, switches and drivers, and an output amplifier. It accepts 2's complement values of input code to produce a negative output. It can be recalibrated to accept 1's complement input.

Either voltage or current output is available, both with 0.1% maximum error referred to reference source, over the full temperature range. The voltage output is obtained by feeding the current output into an IC operational amplifier, provided on the board, which has a full scale output of ±10v and can drive a 20 ma resistive load with 5,000 pf of parallel capacitance.

Input logic levels are standard T Series, 1 unit load per input. The WT49 regulator module is available to provide ±35 volts reference source. Wire the reference voltages and -8v to pins shown in the logic diagram below.

A companion module, the FT58, is available for use as a data register (refer to FT58 description). The FT58 contains two 10-bit buffer registers which may be used as single-rank storage for two DT24's, or double-rank storage for one DT24.

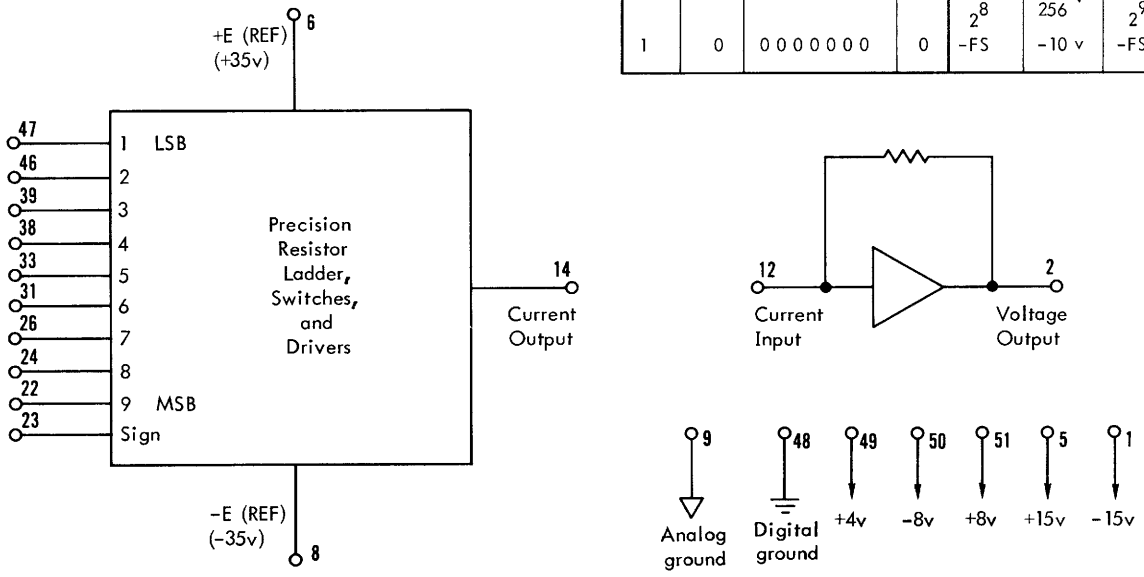
The output voltage is related to digital input as shown in Table 1.

Resolution:	10 bits including sign
Full scale voltage output: (Op. Amp.)	±10 volts
Full scale current output:	±20 ma with Op. Amp., ±4 ma without
Voltage output conversion time:	2.6 µsec per volt of output change (worst case) plus 5 µsec settling time to reach within 10 mv of final value
Current output switching time:	<100 nsec for a transition from + full scale current to - full scale current
Accuracy:	0.1% relative to reference voltage
Temperature range:	0°C to 55°C
Power requirements:	* +35v, 10.5 ma; -35v, 7.5 ma ** +15v, 36 ma; -15v, 36 ma +8v, 73 ma; -8v, 25 ma +4v, 65 ma
Dissipation:	2.2 watts

* From WT49. ** Output Op. Amp. voltages, from PT23.

Table 1. Input vs. Output Relations

DIGITAL INPUT				ANALOG OUTPUT VOLTAGE			
Sign Bit	MSB	2^{-2} 2^{-8}	LSB	2's Complement		1's Complement	
0	0	1 1 1 1 1 1 1	1	$FS-\frac{FS}{2^9}$	$9\frac{502}{512}$ v	$FS-\frac{FS}{2^9}$	$9\frac{502}{512}$ v
0	0	0 0 0 0 0 0 0	1	$\frac{FS}{2^9}$	$\frac{10}{512}$ v	$\frac{FS}{2^9}$	$\frac{10}{512}$ v
0	0	0 0 0 0 0 0 0	0	0	0 v	+0	+0v
1	1	1 1 1 1 1 1 1	1	$-\frac{FS}{2^9}$	$-\frac{10}{512}$ v	-0	-0v
1	1	1 1 1 1 1 1 1	0	$-\frac{FS}{2^8}$	$-\frac{10}{256}$ v	$-\frac{FS}{2^9}$	$-\frac{10}{512}$ v
1	0	0 0 0 0 0 0 0	0	-FS	-10 v	$-FS+\frac{FS}{2^9}$	$-9\frac{502}{512}$ v



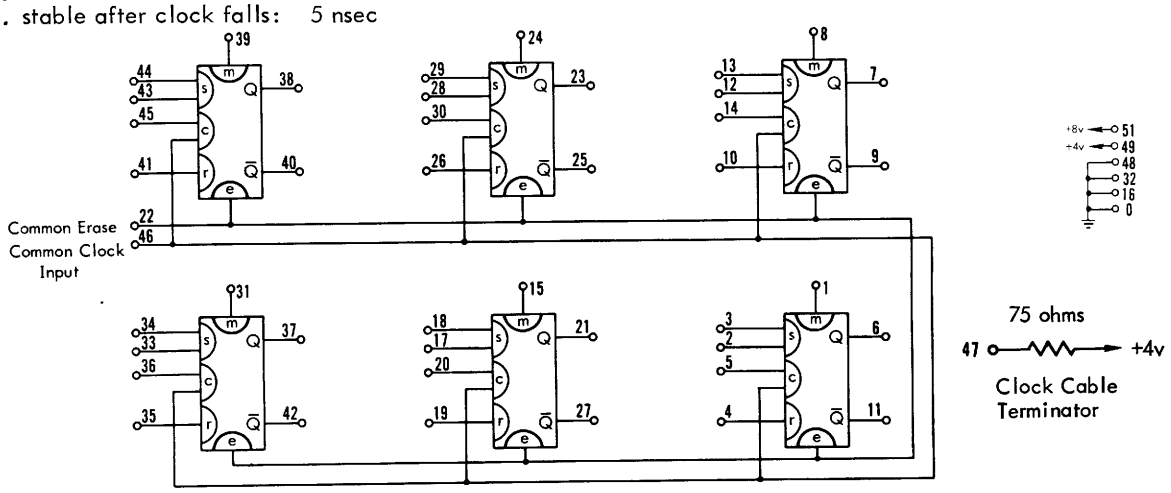
LOGIC DIAGRAM, DT24

FT10

BASIC FLIP-FLOPS

FT10 contains 6 identical flip-flops designed for basic operations as shift registers and binary or BCD counters, either parallel loaded or preset by mark inputs. Terminator is for 33 ohm coaxial clock cable which is used primarily in large computers. Ground m and e if not used.

Maximum Operating Frequency:	10 Mhz
Mark and erase min. True time:	40 nsec
s and r min. stable before clock falls:	30 nsec
s and r min. stable after clock falls:	5 nsec
Clock min. True duration:	30 nsec
Clock min. False duration:	60 nsec
Circuit Delay:	40 nsec typical, 60 nsec worst case
Input Current:	1 Unit load per gate
Fan-out:	14 Unit loads per output
Power Requirements:	+4v, 236 ma av., 360 ma max. +8v, 84 ma av., 107.7 ma max.
Dissipation:	2.53 watts max.



LOGIC DIAGRAM, FT10

FT12

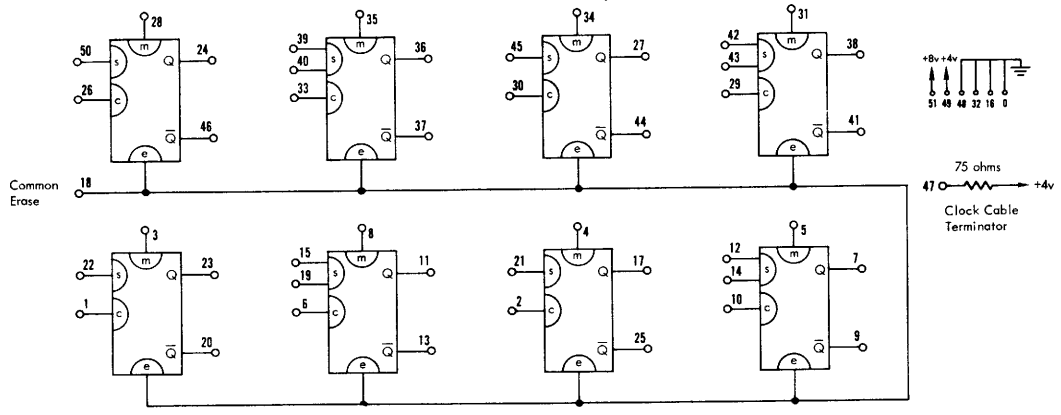
GATED FLIP-FLOPS

FT12, with 8 flip-flop circuits, is designed for applications requiring a large number of economical storage elements on one module. Enough basic gating is supplied for shift registers and binary or BCD counters. Synchronous or bi-directional versions are mechanized by adding gate modules. Reset input is wired True on all 8 circuits (not shown). Since set-1 overrides reset, set input controls reset state.

With external gating this circuit can perform all the functions of two FT11 modules. In many applications it can also take the place of the FT10, at lower cost per flip-flop. Terminator is for 33 ohm coaxial clock cable, primarily used in large computer systems.

Ground mark and erase inputs if not used.

Timing, Input Current, Fan-out same as for FT10.
Power Requirements: +4v, 314.4 ma av., 480 ma max.
+8v, 112 ma av., 143.6 ma max.
Dissipation: 3.37 watts max.



LOGIC DIAGRAM, FT12

4-BIT HIGH SPEED COUNTER

FT11

FT11 contains 4 flip-flops and gating designed for high speed, synchronous counting functions. The module can function as a binary or BCD up- or down-counter, or can be used as a combination counter/shift register. It can be preset at high speed. As with other SDS flip-flop modules, only one logic polarity is required for presetting since set-1 overrides reset. Reset input is permanently wired True, but is not shown in the logic diagram, below.

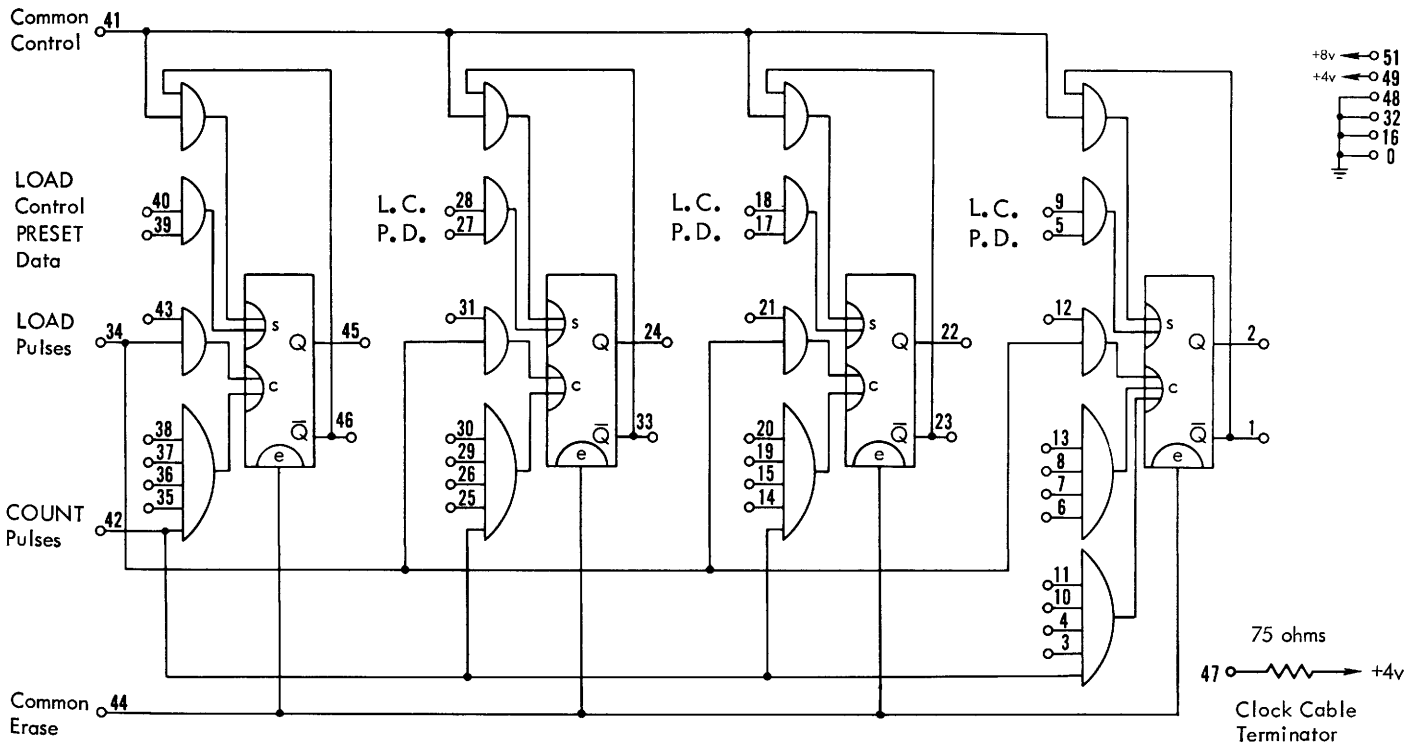
Presetting is accomplished through the 2-input gates marked LOAD Control and PRESET Data. Common Control and COUNT Pulse inputs must be False. Data is entered into the PRESET Data inputs, LOAD Control is made True, and LOAD Pulse is used as a clock. Note that the counter need not be cleared before presetting.

Counting is accomplished with Common Control True, LOAD Control False, LOAD Pulse False, and COUNT Pulse used as clock. The 4-input gates are wired to properly condition the clock inputs for operation in the desired counting or shifting mode, whether binary, BCD, etc.

Common dc reset (without clock) is accomplished with the Common Erase input. This input must be False (ground) when not used.

Terminator is for use with 33 ohm coaxial clock cable, primarily used in large computers.

Max. Operating Freq:	10 Mhz
Timing and Delay:	See FT10 specifications
Input Current:	1 Unit Load per gate input
Fan-Out:	14 Unit Loads, pins 45, 24, 22, 2; 13 Unit Loads, pins 46, 33, 23, 1
Power Requirements:	+4v, 157.4 ma av., 240.2 ma max. +8v, 58.9 ma av., 75.4 ma max.
Dissipation:	1.72 watts max.



LOGIC DIAGRAM, FT11

FT19

MULTIPURPOSE COUNTERS/REGISTERS

The FT19 contains two independent groups of four flip-flops each. With external connections as listed in the table below the module can function in these modes:

1. Storage and Control - data read in and out in parallel
2. Counter, presetable: binary up, binary down, BCD up, and binary up-down (no loss during mode change)
3. Shift Register: all combinations of serial, parallel in/out
4. Shifting Up-Down Counter (accumulator)
   a. Load by: parallel entry, shift in, or count up
   b. Count up or down as desired
   c. Read out by shifting serially, reading in parallel or counting down (no loss during mode change)

It is also possible to form dual 4-bit combinations because the module contains control lines for each group of 4 bits:

1. Two 4-bit counters (binary or BCD) or shift registers
2. One 4-bit up-counter and one 4-bit shift register
3. One 4-bit shifting up-counter (accumulator), one 4-bit shift or store, or one 4-bit up-counter.

Fan-Out: 14 Unit Loads (53.2 ma), pins 3, 5, 25
13 Unit Loads (49.4 ma), pins 31, 7, 27
12 Unit Loads (45.6 ma), pins 41, 43, 37, 39, 35, 21, 23, 13, 17, 9

Power Requirements: +4v, 314 ma av., 480 ma max.
+8v, 157 ma av., 201 ma max.

Dissipation: 3.88 watts max.

For clock and timing specifications refer to FT10

		CONNECTIONS OR LOGIC LEVEL REQUIRED					
CONTROL	PINS	GENERAL STORAGE	SHIFT REGISTER	COUNT UP BINARY	COUNT DOWN BINARY	COUNT U-D BIN., REVERSE	COUNT UP BCD
Count 1, Count 2	42, 12	F	F	T	T**	External logic**	T
Shift 1, Shift 2	38, 8	F	T	F	F	F	F
Up 1, Up 2	24, 14	F	F	T	F	T up, F down	T
Down	50	F	F	F	T	T down, F up	F
Clock	30, 6	Reset input	Shift pulse in	F	F	F	F
Q in 1	44	D	Serial data in	Input	D	Up input	Input 1
$\bar{Q}$ in 1	46	D	D	D	Input	Down input	D
Q in 2	20	D	Q4 (pin 25)*	Q4 (pin 25)*	D	Q4 (pin 25)	Input 2
Common Reset	45	T †	T †	T †	T** †	External logic** †	T †
Mark (dc set)	19, 15, 11, 47, 33, 36, 26, 1	40 nsec T pulse to preset with 1	40 nsec T pulse to preset with 1	40 nsec T pulse to preset with 1	40 nsec T pulse to preset with 1	40 nsec T pulse to preset with 1	40 nsec T pulse to preset with 1
Jumper these pins with wire on back panel:		None	None	Same jumpers for all binary counters: 27-28, 5-4, 31-34, 7-10			41-34, 21-10, 27-40, 5-18, 37-22, 13-2, 31-28, 7-4

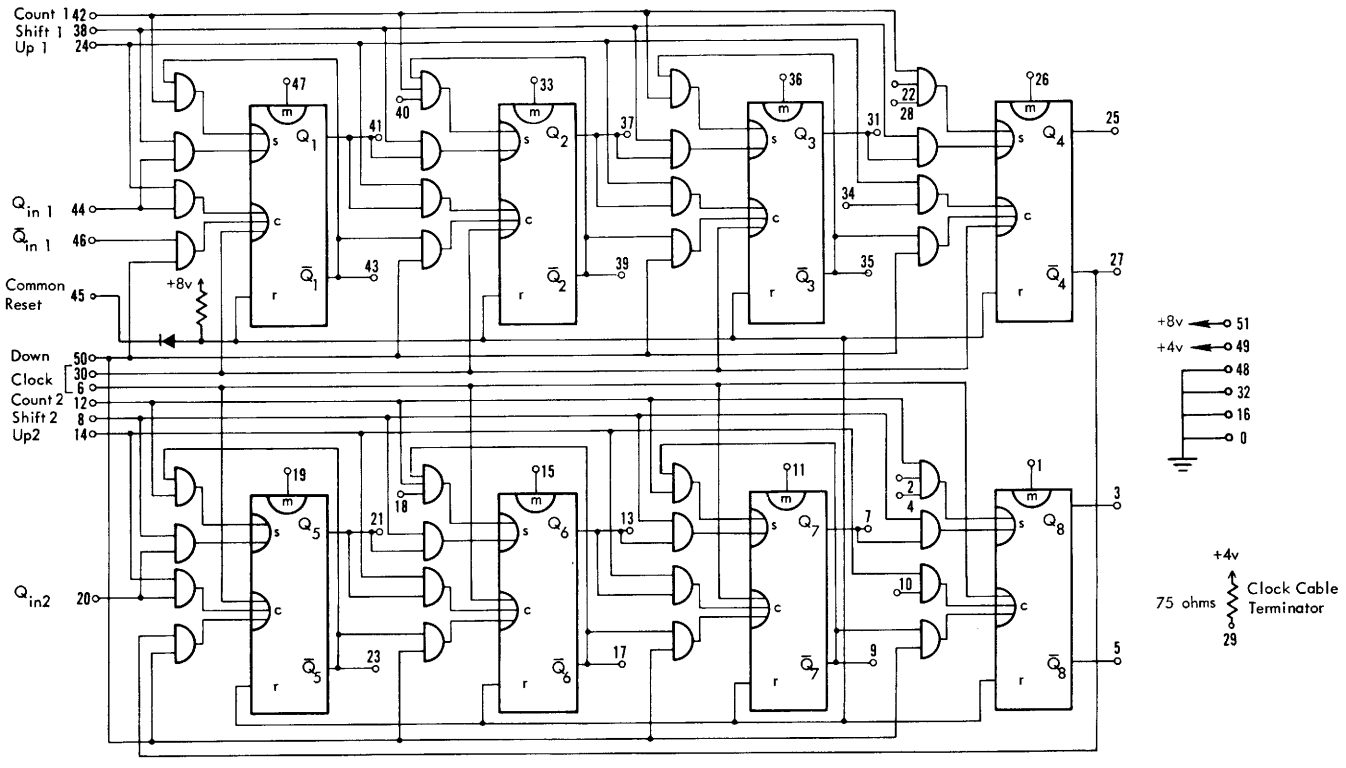
NOTES

F = False (0v, ground)
T = True (+4v, or leave open)
D = don't care (T or F is ok)

* Connect Q4 to Qin 2 to form 8-bit unit. When two 4-bit units are desired use Qin 2 as second input.

** Use 0v (F) pulse to inhibit count and common reset lines when presetting in the down mode or when changing direction with up and down lines. Start the inhibit pulse 30 nsec before changing up and down lines.

† To clear all flip-flops in any configuration, place +4v (T) on common reset (pin 45); place 0v (F) on count, shift, up, and down lines; pulse clock lines with +4v (T), 30 nsec min.



NOTE: 1. Mark inputs must be grounded when not in use. 2. Subscripts refer to ckt. number. Example: Up 2 is Up control line for ckt. 2
3. Clock terminator is for use with 33 ohm coaxial cable. Do not use when clock is brought in by logic wiring.

LOGIC DIAGRAM, FT19

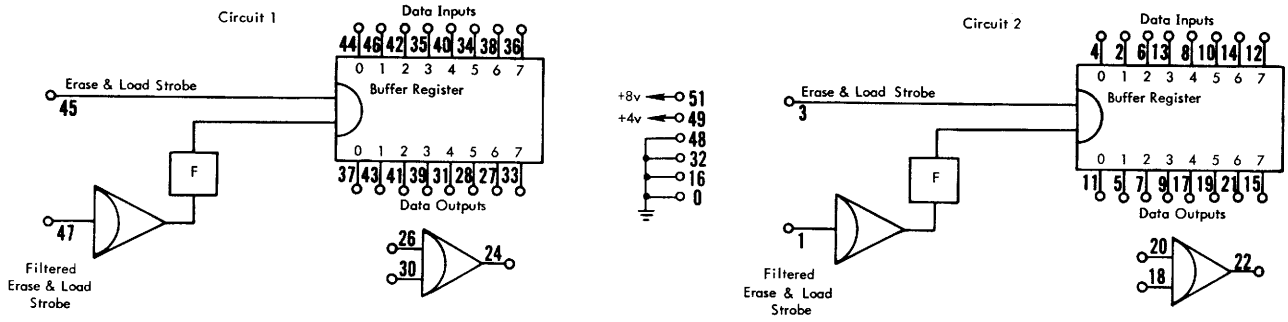
8-BIT BUFFERED LATCH REGISTERS

FT20

The FT20 contains two independent 8-bit buffered latch registers, useful for low cost storage. Data is loaded and read in parallel. Only one strobe, minimum 70 nsec. True, is needed to both erase and update contents. When strobe goes high data inputs must remain stable until 100 nsec after strobe leading edge has risen to within 20% of final value. Outputs can be read after 90 nsec following strobe leading edge.

A filtered strobe is provided for use in noisy environments. Filtered strobe must be True for 200 nsec minimum. Output is then available 300 nsec after strobe leading edge.

Output Drive:	13 Unit Loads per output
Power Requirements:	+4v, 247 ma av., 385 ma max.
	+8v, 62 ma av., 79 ma max.
Dissipation:	2.39 watts max.



LOGIC DIAGRAM, FT20

T SERIES Modules In SDS SIGMA 7 Computer. Note use of Front-edge Cable Connectors.

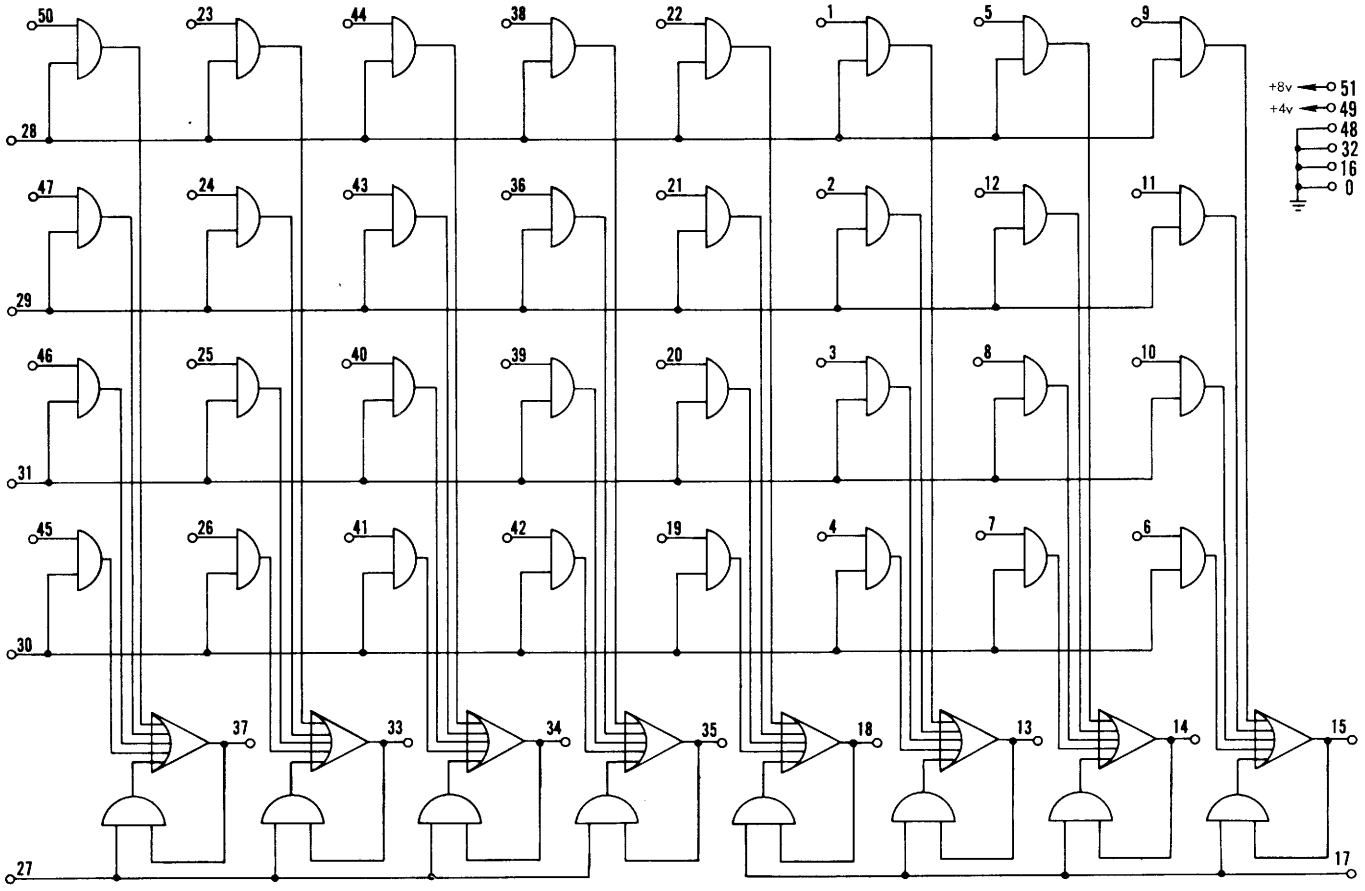
FT26

BUFFERED LATCH MULTIPLEXING MATRIX

The FT26 module contains 8 circuits which can be used individually as buffered latch circuits. The entire module can also be used for digital multiplexing.

Each circuit can be used as a latch circuit preceded with a 4-input OR, by leaving pins 28, 29, 30, and 31 open (True) while using pins 17 and 27 as latch control inputs. The module can be used as a 4 x 8 buffered digital multiplexing matrix with optional latch storage by wiring pins 28, 29, 30, and 31 as multiplex controls and pins 17 and 27 as latch controls. Other applications may be devised.

Fan-Out, each buffer output: 13 Unit Loads (49.4 ma)
Power Requirements: +4v, 95 ma av., 156 ma max.
+8v, 112 ma av., 144 ma max.
Dissipation: 1.95 watts max.



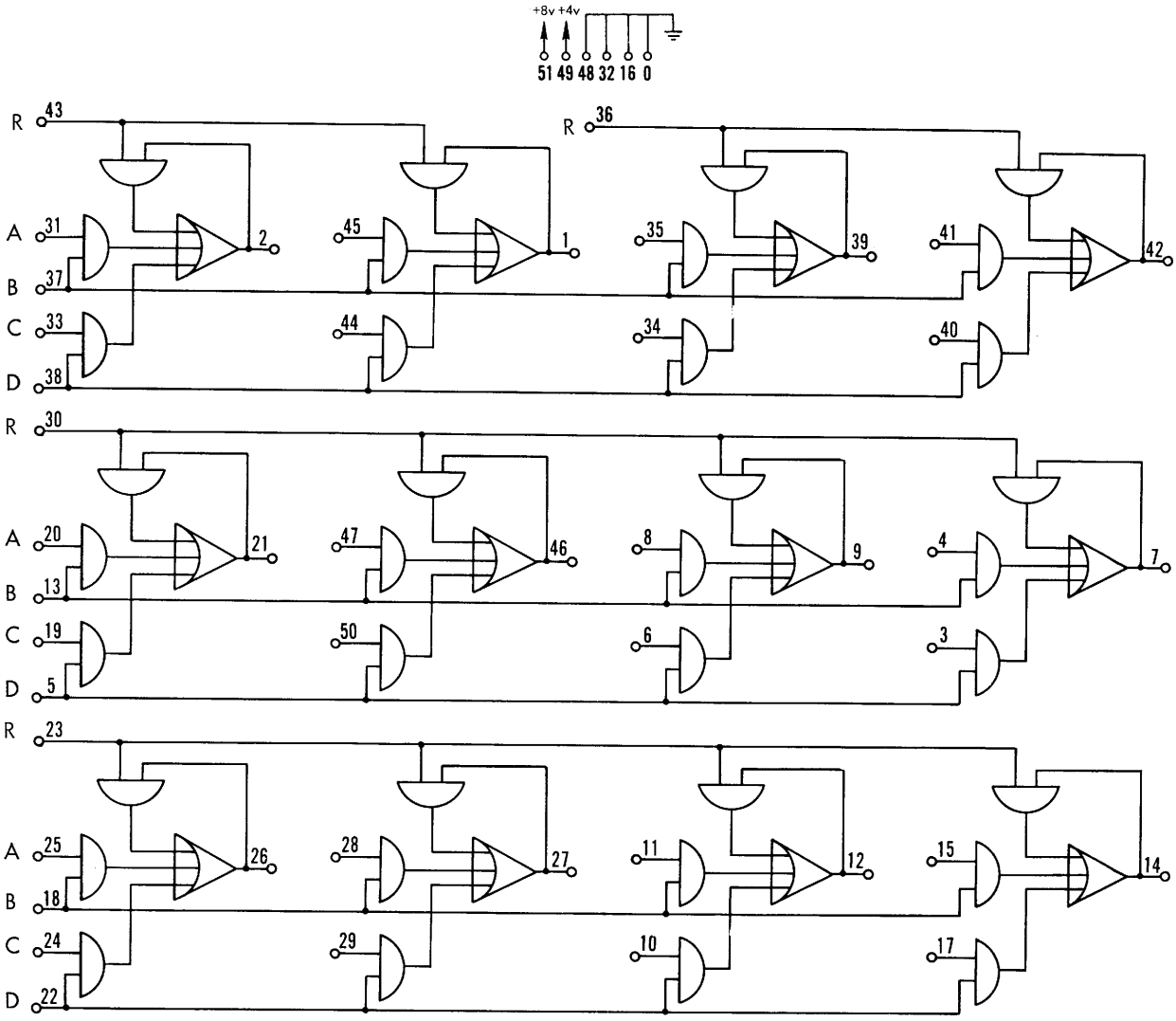
LOGIC DIAGRAM, FT26

BUFFERED LATCHES

FT27

FT27 contains 12 latching circuits for use as unclocked storage elements. Each latch circuit has two gated inputs shown in the diagram below as A·B + C·D. B and D are each common to 4 latches and can be used as common control lines. Input R is the latching input. When R is True and A·B or C·D is True, the buffer output goes True and remains True until R goes False. This circuit provides a low cost memory capability and can be used in applications where the fully buffered output of the T Series flip-flop is not required.

Power Requirements: +4v, 142 ma av., 234 ma max.
+8v, 101 ma av., 129 ma max.
Dissipation: 2.17 watts max.



LOGIC DIAGRAM, FT27

FT40

FAST ACCESS MEMORY

The FT40 fast access memory module provides storage of 128 bits on one module, arranged as sixteen 8-bit bytes. Up to 32 modules can be operated with one set of address lines, giving a memory size of 32 x 128 = 4,096 bits.

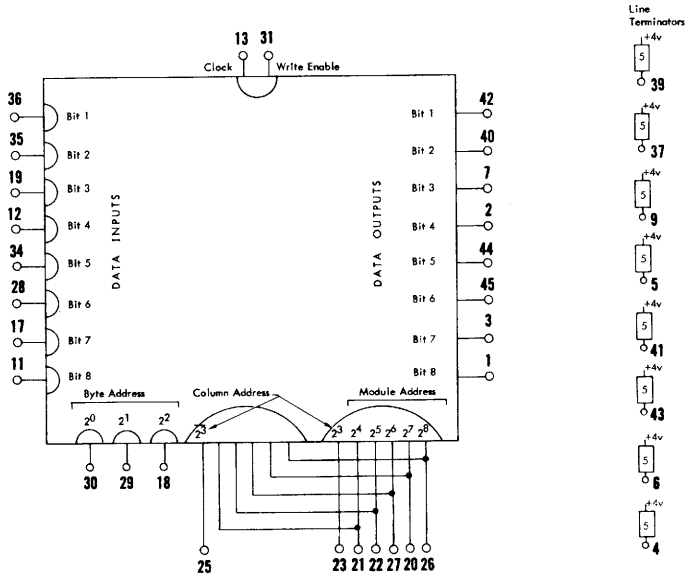
The FT40 reads and writes significantly faster than a core memory. Typical core access time is greater than 700 nsec, while the FT40 has a write time of 165 nsec or less and a read time of 110 nsec or less. The module interfaces directly with other T Series modules, requiring no special read-write electronics or power supplies.

The FT40 costs less per bit than standard flip-flop storage. This makes it attractive for use in long shift registers or peripheral equipment input-output buffers and similar large data capacity applications.

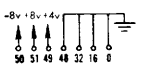
The FT40 is operated as follows (refer to the logic diagram). Data is written in or read out 8 bits at a time. The module is addressed when all five Module Address lines, 2^4 through 2^8, are True. If any one of these five Module Address lines is False all Data Outputs are True, but may be pulled False by a Data Output line from another FT40 wired in parallel. There are 16 storage locations, each holding one 8-bit byte, on each FT40. Data is read out of any one of these 16 locations by addressing the Byte Address, 2^0, 2^1, and 2^2, and the Column Address, 2^3 and $\overline{2^3}$. Readout is nondestructive. Data is written in to any one of these 16 locations on the trailing edge of clock, by addressing the locations (2^0, 2^1, 2^2, 2^3, $\overline{2^3}$) and holding Write Enable True.

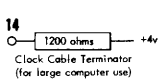
The line terminators (220 ohms each) are used as pull-up resistors for the data output lines. No pull-up resistors are connected on the module to the data outputs. Up to sixteen data output lines can be connected together and returned to +4 volts through one 220 ohm resistor. A 1200 ohm clock cable terminator is also provided on the module for use in large systems where clock (write pulse) is distributed via 33 ohm cable, and the cable is terminated by thirty-two 1200 ohm resistors in parallel. In smaller systems, where timing skew is not a critical factor, ordinary logic wiring can be used to deliver the clock pulse to each module.

Input Logic Levels:	Logic 1: +4v Logic 0: 0v
Output Logic Levels:	Logic 1: +4v Logic 0: 0v
Fan-out (each output):	11 Unit loads (42 ma) with 220 ohm pull-up resistor connected
Load imposed by each logic input:	Pins 20, 21, 22, 26, 27: 2 unit loads; all others 1 unit load
Circuit Delay:	Read: 110 nsec worst case (60 nsec typical) Write: 165 nsec worst case (90 nsec typical)
Write Control Conditions: (worst case)	Address, Data, and Write-enable should be stable 80 nsec before clock leading edge, and remain stable 45 nsec after clock trailing edge. Minimum clock pulse: 40 nsec.
Read Control Conditions:	Address should be stable 110 nsec before outputs are read.
+4 Volt Supply:	1.28 amp max. (550 ma typical)
+8 Volt Supply:	146 ma max. (63 ma typical)
-8 Volt Supply:	2 ma
Module Dissipation:	6.25 watts max. (2.7 watts typical)
Temperature Range:	+5°C to +50°C with convection cooling +5°C to +70°C with forced air cooling, 100 linear fpm airflow (use ZT20)



LOGIC DIAGRAM, FT40



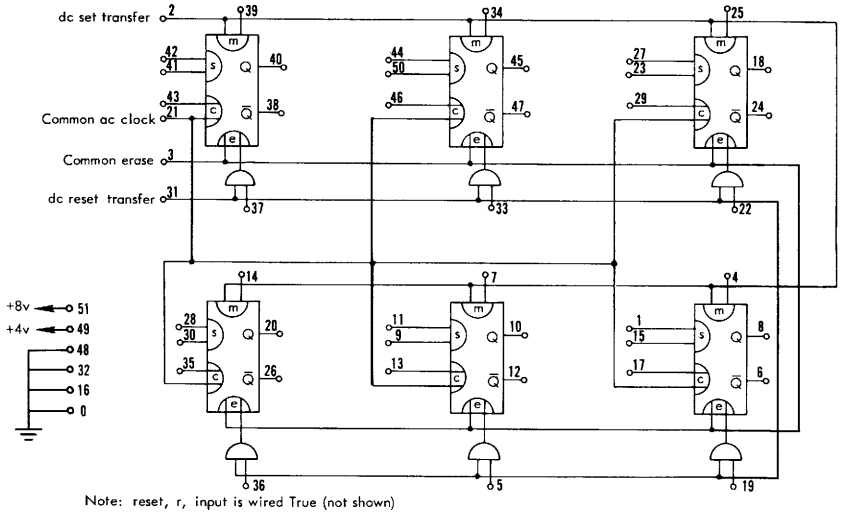


STANDARD FLIP-FLOPS

FT43

The FT43 contains six flip-flops having separate, gated mark and erase inputs for each flip-flop. Separate and common clock inputs are provided. Reset inputs (not shown) are wired True. The flip-flop is controlled via the set input in clocked applications. The circuit has many uses. For example, all gating is provided for a jam-transfer register. The OR'ed clock permits multi-function applications such as combination ripple-counters/shift registers.

Power Requirements:	+4v, 236 ma av., 360 ma max.
	+8v, 151 ma av., 194 ma max.
Dissipation:	3.29 watts max.



Note: reset, r, input is wired True (not shown)

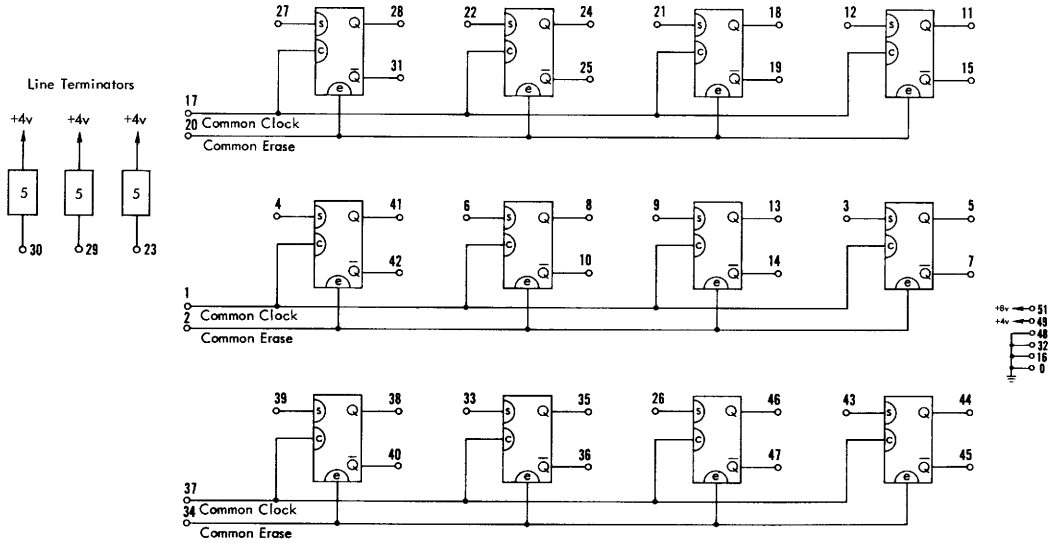
LOGIC DIAGRAM, FT43

CLOCKED FLIP-FLOPS

FT56

The FT56 contains twelve economical flip-flops, in three groups of four. Each group of four has a common clock input line. All reset inputs are wired True. Flip-flop states are controlled by using the set input, since set True overrides reset True. Three 220 ohm line terminators are also provided. No mark inputs are provided.

Power Requirements:	+4v, 470 ma av., 720 ma max.
	+8v, 134 ma av., 172 ma max.
Dissipation:	4.69 watts max.



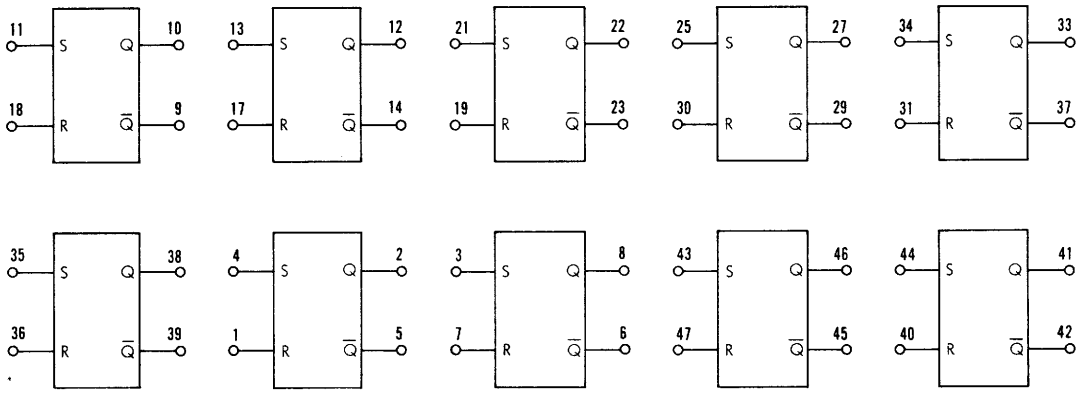
LOGIC DIAGRAM, FT56

FT57

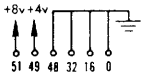
DC (RS) FLIP-FLOPS

The FT57 module contains ten dc flip-flops (cross-coupled NORs) for use where the buffered outputs and the clocked inputs of the SDS 307 IC flip-flop are not required. These flip-flops may be economically used in storage registers, as control flip-flops, etc.

Min. True Pulse:	20 nsec.
Power Requirements:	+4v, 218 ma av., 390 ma max.
	+8v, 112 ma av., 144 ma max.
Dissipation:	2.98 watts max.



LOGIC DIAGRAM, FT57



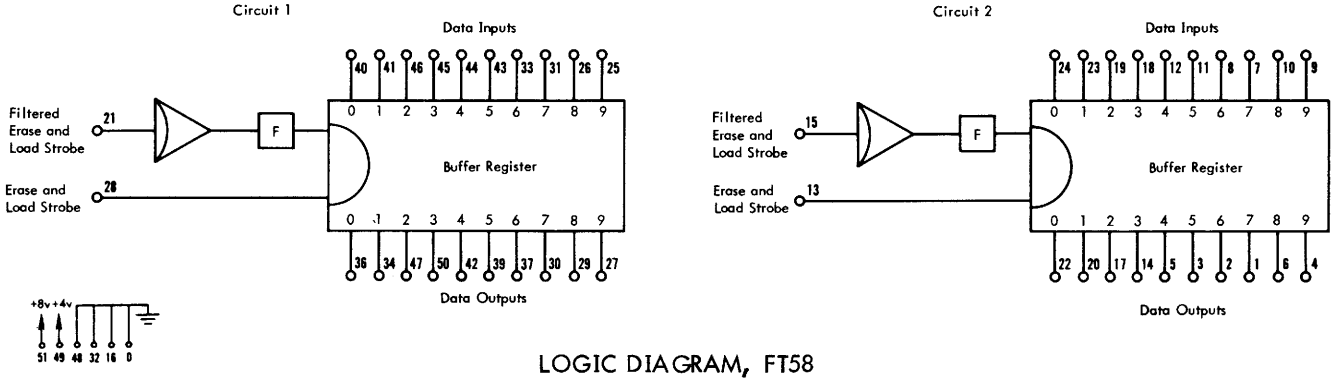
FT58

FLIP-FLOPS 10-BIT BUFFERED LATCH REGISTERS

The FT58 contains two independent 10-bit buffered latch registers, useful for low cost storage. Data is loaded and read in parallel. Only one strobe, minimum 70 nsec True, is needed to both erase and update contents. When strobe goes high, data inputs must remain stable until 100 nsec after strobe leading edge has risen to within 20% of final value. Outputs can be read after 90 nsec following strobe leading edge.

A filtered strobe is provided for use in noisy environments. Filtered strobe must be True for 200 nsec minimum. Output is then available 300 nsec after strobe leading edge.

Max. Operating Freq.:	Depends on strobe timing
Output drive:	13 Unit Loads per output
Power requirements:	+4v, 321 ma av., 531 ma max.
	+8v, 140 ma av., 180 ma max.
Dissipation:	3.92 watts max.



LOGIC DIAGRAM, FT58

UNIVERSAL OPERATIONAL AMPLIFIER

HT58

The HT58 is a fast, high-input impedance, high-output current, differential amplifier with provisions for adjustment of gain and zero offset. In addition, the input offset voltage temperature coefficient is adjustable.

A feature of the amplifier is a front-end shield plane, driven from the common mode point, and an electrical "FET Guard", which reduces the effective input capacity when used in the buffer mode. Pins adjacent to the inputs are also driven to eliminate effects of stray capacitance. This signal may be used for external guards if desired.

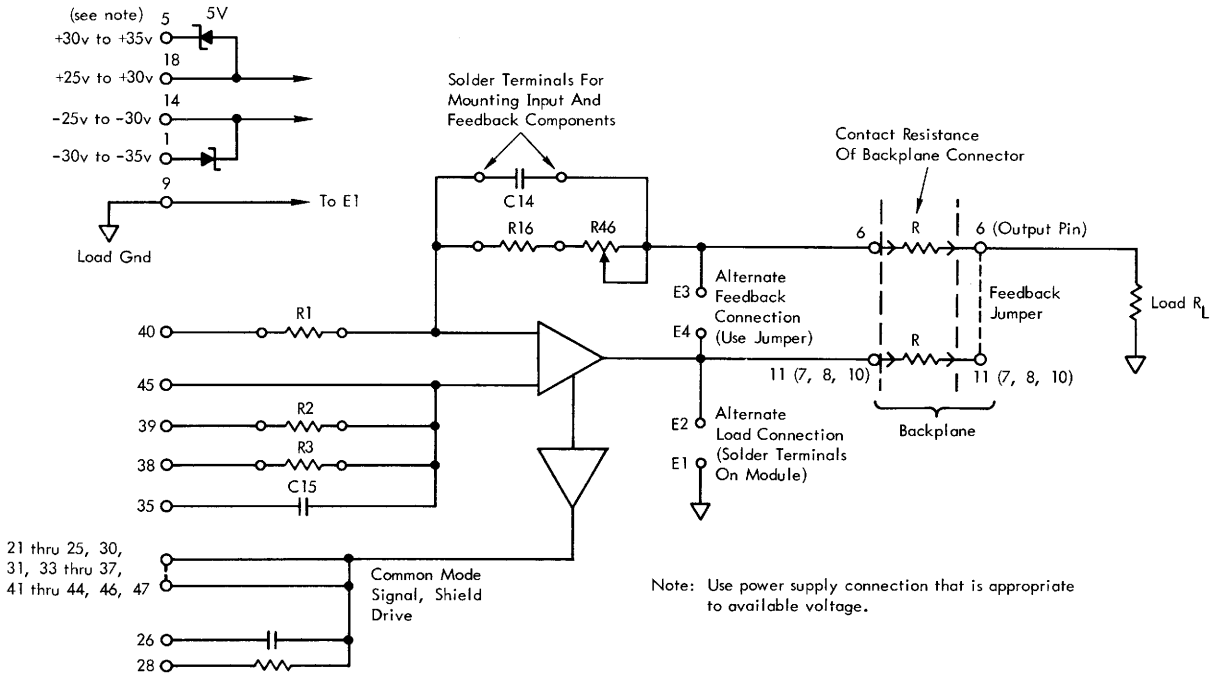
The amplifier is available in a variety of popular gain configurations (see Tables 1, 2, 3). Other resistor configurations may be obtained on special request. In addition, a unit is available without gain resistors or gain pot.

Input

Open loop gain:	$.5 \times 10^6$
Zero drift:	±10 μv/°C (easily adjustable)
Common mode rejection:	100 db, dc; 60 db, 1KHz (Resistor error may be adjusted out)
Input impedance (buffer mode):	Junction FET typically paralleled by less than 1 pf capacitance
Input bias current (FET leakage):	.1 nanoamp at 25°C; 1 n.a. at 55°C
Input voltage range:	±10 volts divided by the closed loop gain (min. 1, max. 10)
Recovery time from 10X overvoltage: (not to exceed common mode of ±15v on either input)	OP Assy's and Diff. Amp.: 10 μsec Buffer: 12 μsec.

Output

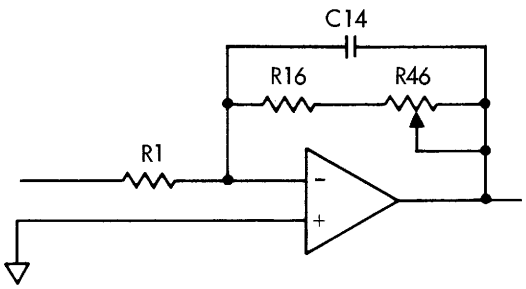
Voltage swing:	±10 volts
Current:	±40 ma. (self limiting)
Output impedance:	.01 ohm max. at D.C., all configurations; 1 ohm max at 1 MHz, unity gain (proportional to gain)
Min. load impedance:	250 ohms || 2,000 pf
Settling time to within 1 mv of final value:	5 μsec, at unity gain, full load (+10v to -10v or -10v or +10v)
Slew rate:	10v/μsec., typical
Noise (Wideband):	.5 mv. p-p RTO
Output connections:	Either at solder terminals on board or at connector pin (with feedback jumpered). See General Configuration.
Power Supply Voltage:	Pins 18 & 14, +(25 thru 30)v and -(25 thru 30)v or pins 5 & 1, +(30 thru 35)v and -(30 thru 35)v
Power supply current:	25 ma. plus load current
Power supply recommended:	PT24



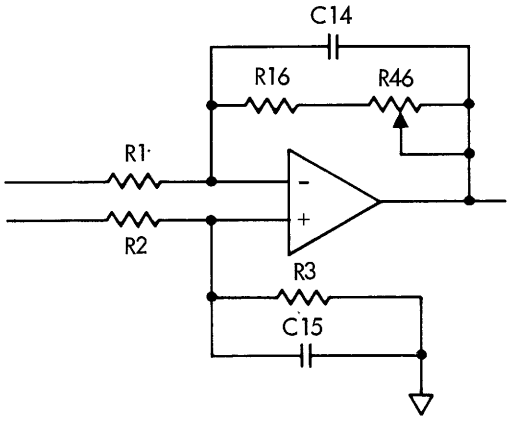
Note: Use power supply connection that is appropriate to available voltage.

GENERAL CONFIGURATION, HT58

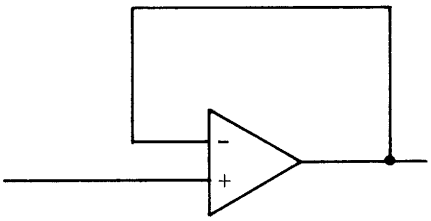
Operational Amplifier



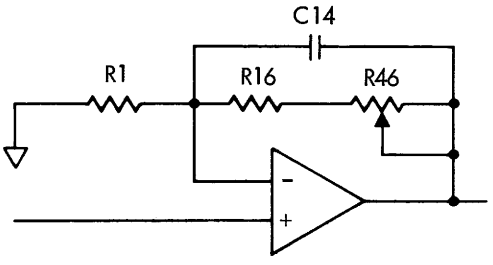
Differential Amplifier



Unity Gain Buffer



Buffer With Gain



Popular Gain Configurations, HT58

Table 1. Operational Amp. Configurations

④ Dash No.	R1	R16 + R46	① C14	R2	R3	Gain	Settling Time ② µsecs
-1	10K	10K	10PF	-	-	X1	5
-2	10K	100K	5PF	-	-	X10	10
-3	100K	100K	5PF	-	-	X1	10
-4	Short	2.5K	10PF	-	-	③	5

Table 2. Differential Amp. Configurations

Dash No.	R1	R16 + R46	C14	R2	R3	Gain	Ts
-5	10K	10K	10PF	10K	10K	X1	5
-6	10K	100K	5PF	10K	100K	X10	10
-7	100K	100K	5PF	100K	100K	X1	10
-8	-	-	-	-	-	-	-

Table 3. Buffer Configurations

Dash No.	R1	R16 + R46	C14	R2	R3	Gain	Ts
-9	-	-	Short	-	-	X1	5
-10	1K	9K	10PF	-	-	X10	10

① May be tailored for specific applications.

② 20v swing on output, settling to within 1 mv of final value.

③ ±4 ma input current produces ∓ 10v output.

④ Order configuration desired by dash no. suffix. Example: HT58-6 is second configuration listed in Table 2.

VOLTAGE COMPARATORS

HT72

The HT72 contains two general purpose operational amplifier circuits, designed for applications not requiring the performance of the HT58 amplifier. This module uses two integrated circuit linear amplifiers, with additional components, which provide two major improvements:

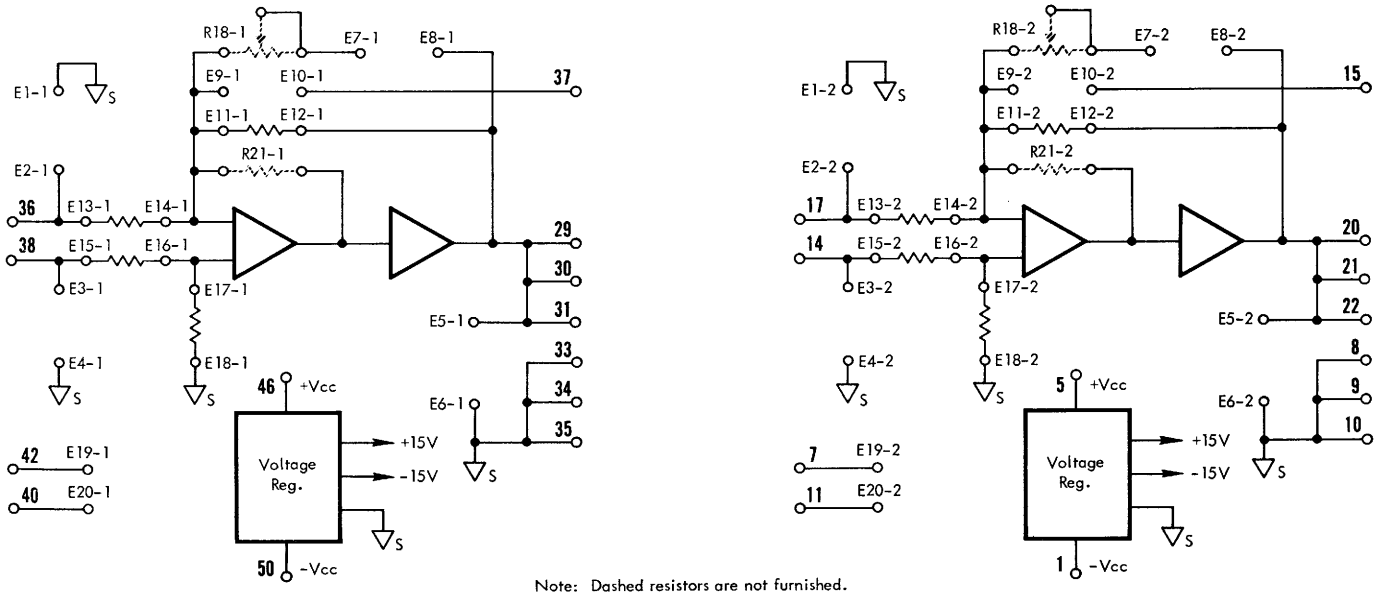
1. Additional power amplification produces greater output current (20 ma at 10v).
2. An internal supply voltage control allows broader tolerance in supply voltage (±20%). The internal voltage control assures that gain is stable in spite of supply voltage changes.

Differential or unipolar input may be used. Output is single-ended. Configurations available are similar to those of the HT58 module (refer to HT58 description). Due to the excellent gain stability, accuracy of the amplifier depends primarily on feedback resistor accuracy. The amplifier is provided with 1% feedback resistors, mounted on standoff terminals, which result in overall accuracy better than 1.4%. If these are replaced with 0.01% resistors, at user option, accuracy will be better than 0.1%.

Additional standoff terminals are provided on the module, which allow the user to modify the feedback of the amplifier by adding components.

Characteristic	Units	Min.	Typ.	Max.
Input				
Open loop gain		12,000	45,000	
Temp. coefficient of input offset voltage*	μv/°C		6	
Input impedance	Kohms	150	400	
Input bias current	μamp.		0.5	2.0
Input offset current	nanoamp.		100	750
Input voltage range	volts			±10
Differential input voltage range	volts			±5.0
Output				
Voltage swing	volts			±10
Current	ma			20
Output impedance (open loop)	ohms	22	30	50
Power supply voltage	volts	20	25	30
Power supply current	ma	25		90
Dissipation, per module	watts	0.50		2.7

* The total offset of the amplifier is adjustable to within ±300 μvolts.



Note: Dashed resistors are not furnished.

LOGIC DIAGRAM, HT72

HT73

VOLTAGE COMPARATORS

The HT73 module contains nine independent logic circuits with differential inputs. When the voltage at the + input becomes more positive than the voltage at the - input by a predetermined comparison value the output goes to logic 1 (high) level. The comparison level is determined by the resistor and Vref connections which are made at the - input.

The HT73 is used as a sensitive level detector or interface module. The HT73 uses the same circuit board and amplifies as the AT69 differential receiver.

Comparator sensitivity is better than 10 mv; that is, when the + input becomes 10 mv more positive than the comparison level, the output goes high. The comparison level is the voltage at point P (see connection diagram).

The voltage at comparison point P is usually determined by the combination of V ref and a voltage divider network R3/R5 that can be placed at the - input. The resistor R3 that is provided on the module is a 4.64K ohm, 1% precision resistor. R5 is supplied by the user.

The voltage at the comparison point, P, should not go beyond the range -5v to +5v when supply voltages of ±8v are used for -v and +v. The range at point P can be extended as far as -12v to +12v by raising -v and +v to -15v and +15v.

This voltage divider arrangement permits the use of a relatively high precision reference voltage such as the 35 volts that is available from the WT49 module.

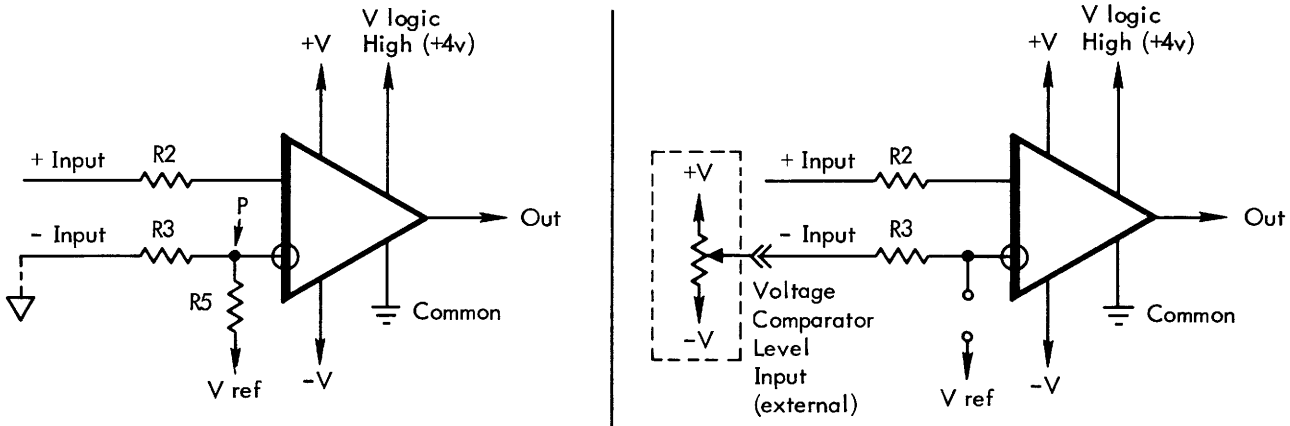
An external variable comparator level input may be substituted as shown in the connection diagram, if an adjustable comparison input is available.

The HT73 output logic level is determined by the supply voltage connected to pin 26. For T Series use pin 26 is tied to +4 volts.

Both input terminals and the Vref terminal are available at front-edge cable connectors (⟶⟫) as well as a backpanel connectors (⊸○).

Max. Data rate:	1 Mhz
Max. input voltage (from + input to ground):	15 volts
Comparison level range (at point P) with	
+v=+8v and -v=8v:	-5v min., +5v max.
with +v=15v and -v=15v:	-12v min., +12v max.
Max. Vref:	Depends on R3 and R5 (refer to text)
Input impedance:	200K ohms min.
Fan-out:	37 Unit Loads
Propagation delay, at 25° C:	170 ns typ.
+4 volt supply (Vcc):	60 ma typ. 68 ma max.
+8 volt supply:	220 ma typ. 270 ma max.
-8 volt supply:	16 ma typ. 25 ma max.
Dissipation, per module:	2.27 watts typ. 3.07* watts max.

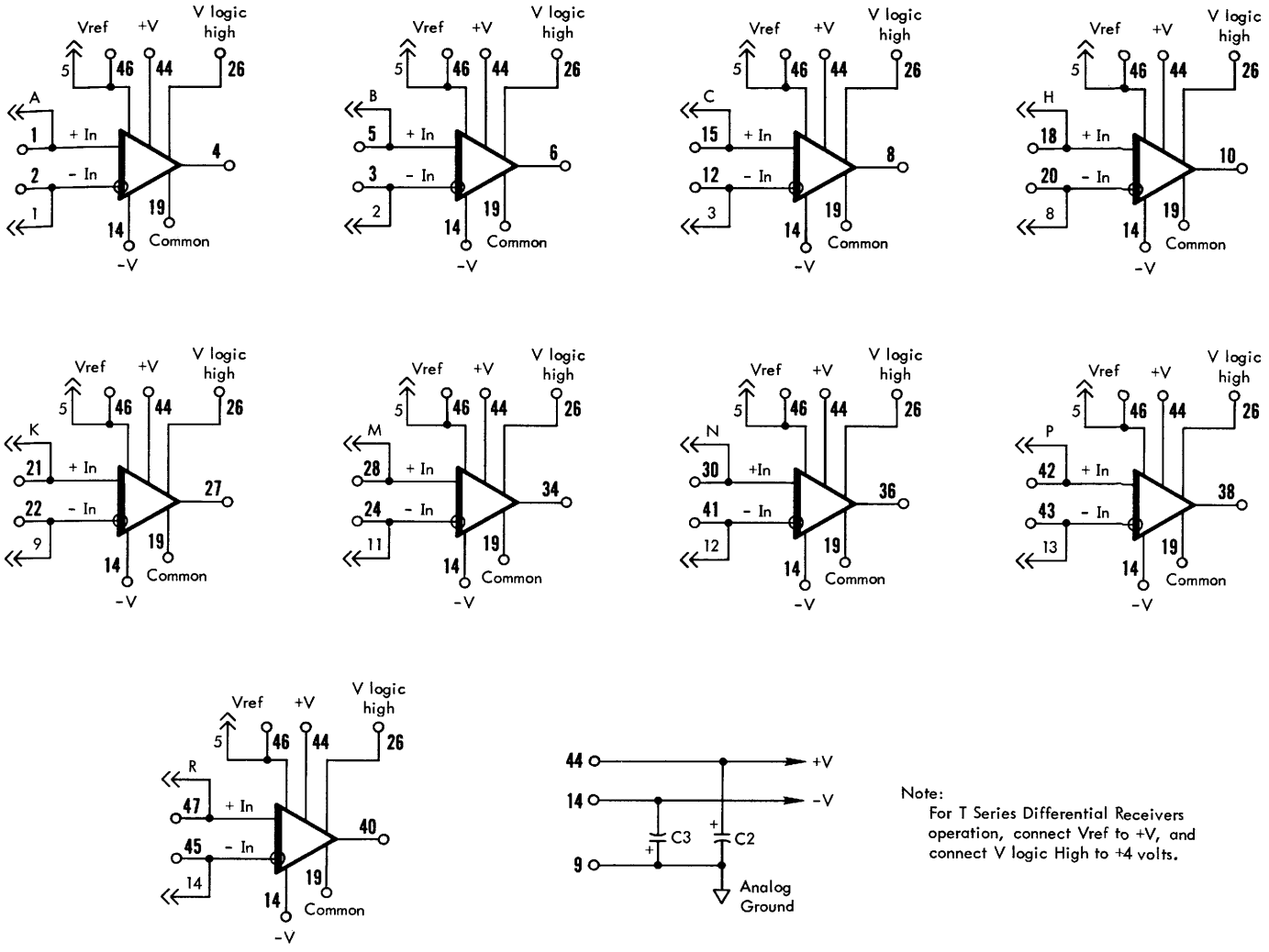
* at 10% overvoltage



With fixed V ref and voltage divider

With voltage comparator level input

HT73 Connection Diagram



Note:
For T Series Differential Receivers operation, connect Vref to +V, and connect V logic High to +4 volts.

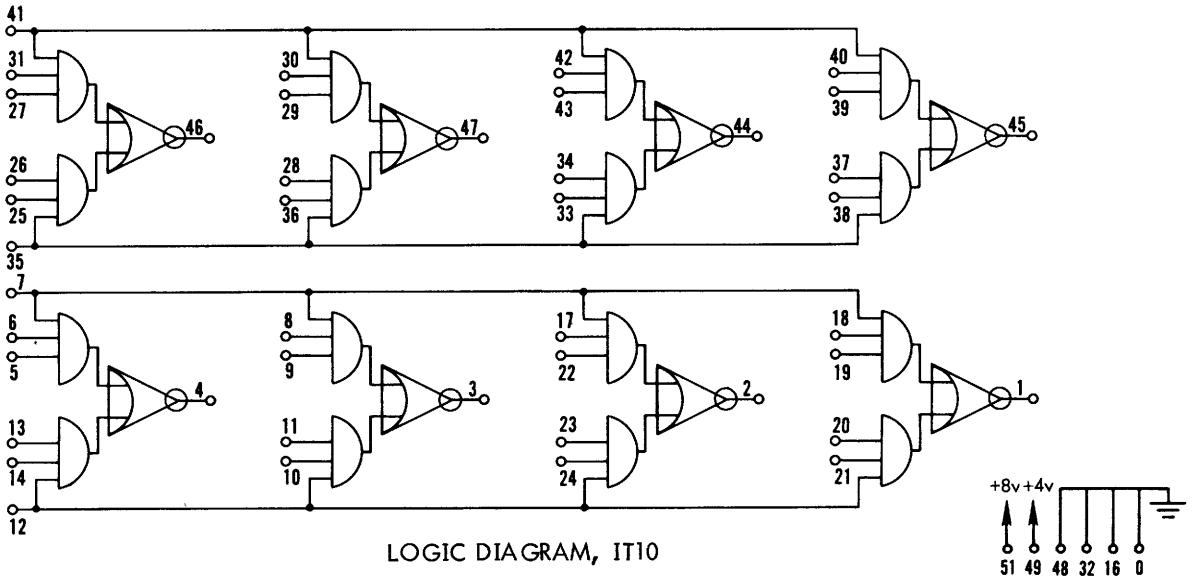
LOGIC DIAGRAM, HT73

IT10

INVERTED AND/OR GATES (AND/NORs)

Eight inverting AND/OR gate structures (AND/NORs) are on these modules. Each circuit consists of two 3-input AND gates, the outputs of which are ORed and inverted. One input on each AND gate is shared with 3 other circuits. The circuits are designed to implement expressions of the type $\overline{A \cdot B \cdot C + D \cdot E \cdot F}$. By connecting IT10 circuit outputs together a larger NOR function can be generated, of the type $\overline{A \cdot B \cdot C + D \cdot E \cdot F + G \cdot H \cdot I + J \cdot K \cdot L}$. Refer to BT10 description for non-inverting versions of these circuits.

Power Requirements:	+4v, 87 ma av., 156 ma max.
	+8v, 45.0 ma max., 57.5 ma max.
Dissipation:	1.2 watts max.



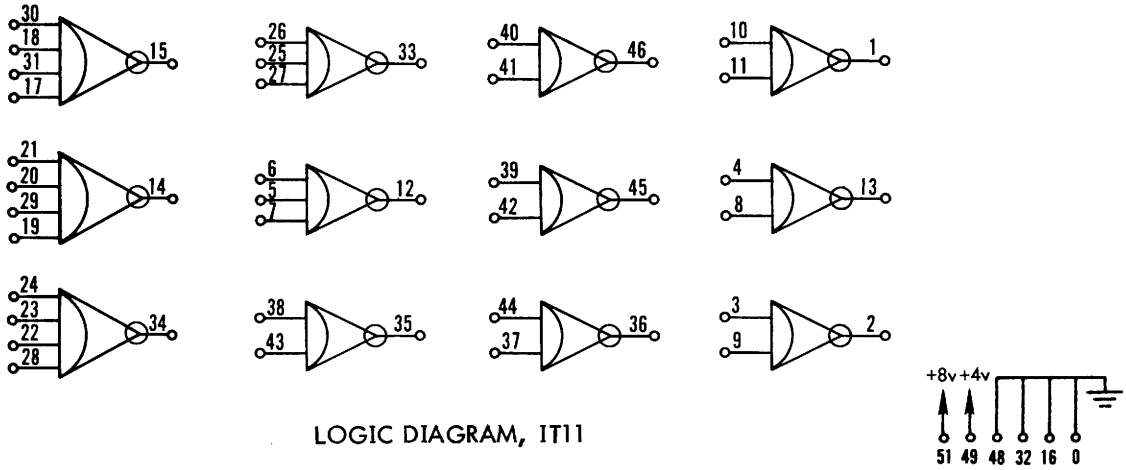
LOGIC DIAGRAM, IT10

IT11

INVERTED AND GATES (NAND GATES)

The IT11 has an assortment of NAND gates for general purpose use. There are two 3-input circuits; three 4-input circuits; and seven 2-input circuits. The NAND functions can be ANDed by connecting outputs together. Refer to BT11 description for the non-inverting versions of these circuits.

Power Requirements:	+4v, 130 ma av., 234 ma max.
	+8v, 33.6 ma av., 43.0 ma max.
Dissipation:	1.45 watts max.



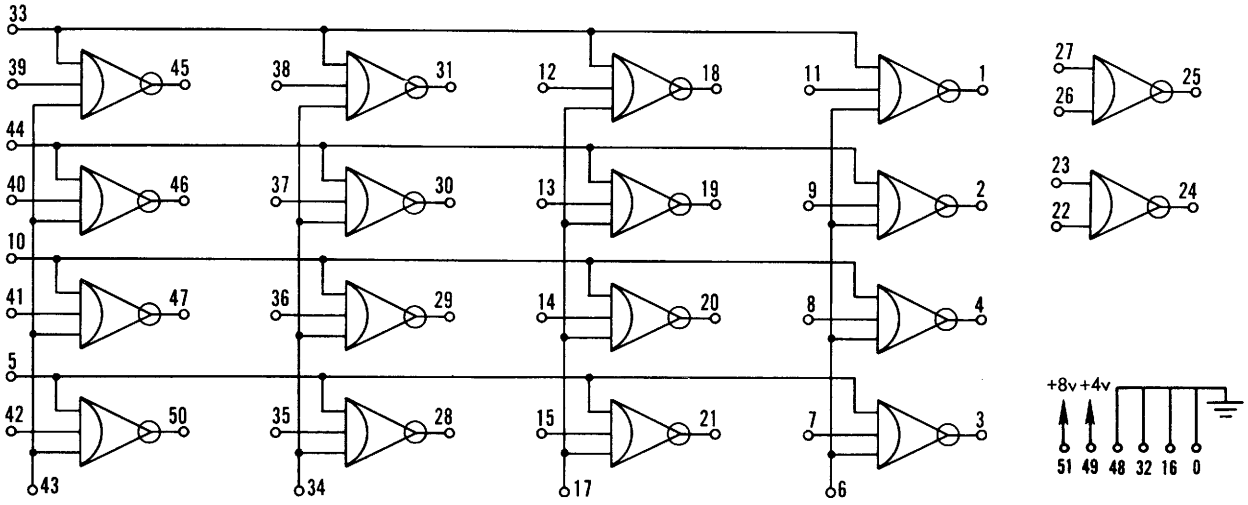
LOGIC DIAGRAM, IT11

INVERTER MATRIX

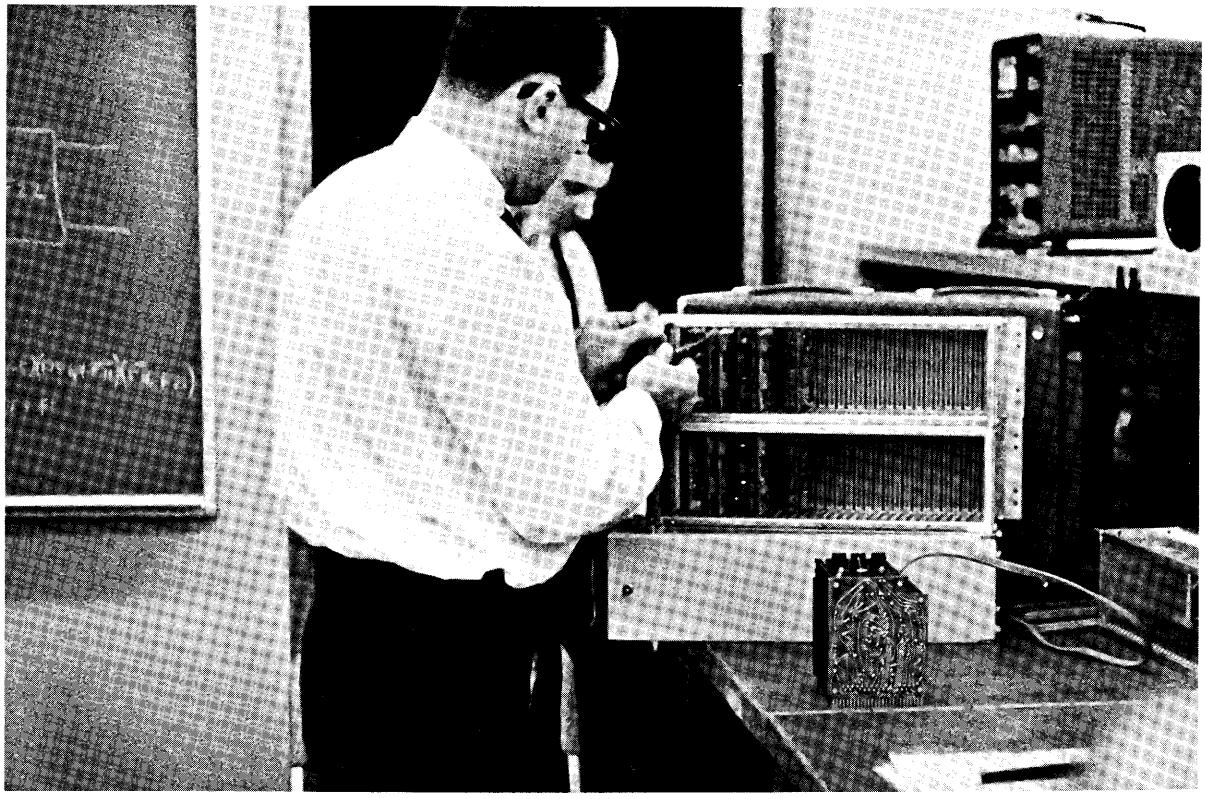
IT13

IT13 has a 4 x 4 matrix which can (1) select one of up to 4 groups of 4 bits each, or (2) generate up to 16 discrete outputs from a 4 x 4 matrix input, or (3) provide 18 general purpose inverters. Gate structure is identical to BT13.

Power Requirements:	+4v, 124 ma av., 219 ma max.
	+8v, 28 ma av., 36 ma max.
Dissipation:	1.07 watts max.



LOGIC DIAGRAM, IT13



IT14

INVERTED AND/OR MATRIX (AND/NOR MATRIX)

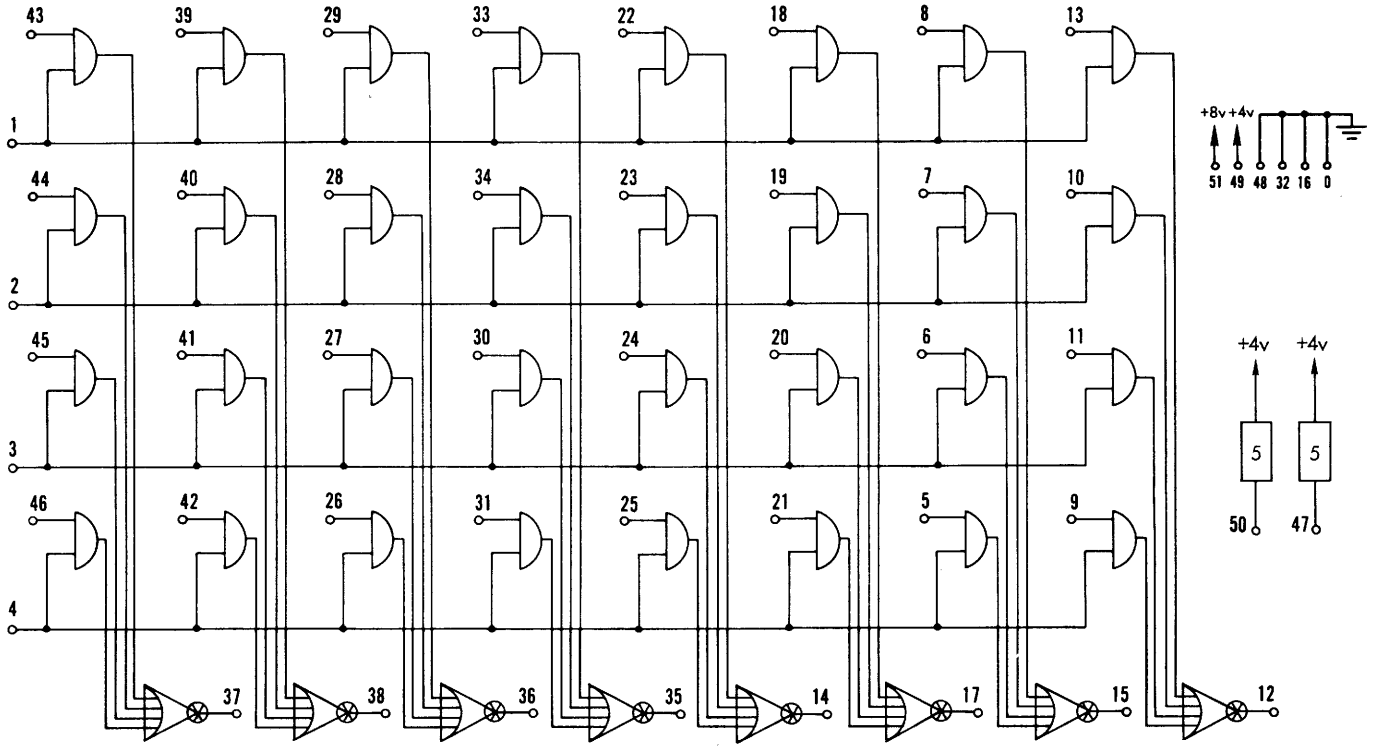
The IT14 module contains a matrix of eight buffered AND/NOR gates (AND/OR-inverters) which have common AND inputs as shown in the logic diagram below. Each gate can be used as an independent 4-input NOR if all common pins are left open (True). The NOR outputs can be tied together to form NORs with more than four inputs. The entire structure can be used as a 4 x 8 digital multiplexing matrix if the common pins are strobed in sequence.

The outputs do not have pull-up resistors connected on the board. This permits formation of wired logic functions without a fan-out penalty, by tying outputs together. However, at least one pull-up resistor must be present on any combination of outputs wired together (or on a single output used alone) to provide the high logic level for the gates connected to the output(s). If no pull-up resistor is present, connect one of the two 5-unit-load terminating resistors supplied on the module. Additional terminators are available on the XT10 module.

The structure of the IT14 is similar to that of the FT26.

Power Requirements:	+4v, 67.6 ma av., 96 ma max.*
	+8v, 90 ma av., 115 ma max.
Dissipation:	1.21 watts max. +pull-up power

*Add current drawn by output pull-up resistors, at 3.8 ma per unit load.



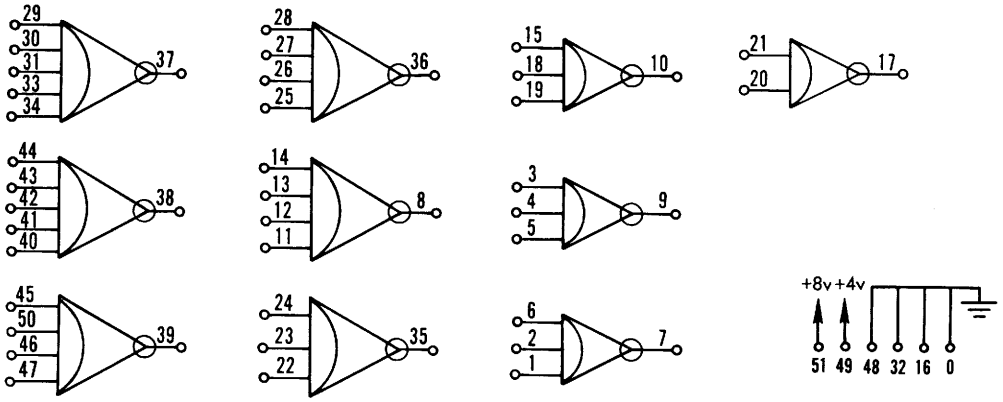
LOGIC DIAGRAM, IT14

INVERTED AND GATES (NAND GATES)

IT18

The IT18 module contains ten NAND circuits intended for general purpose use. Each circuit can drive 14 loads. Outputs may be paralleled with other circuits; each paralleled output decreases the output drive capability by 2 unit loads.

Power Requirements:	+4v, 124 ma av., 219 ma max.
	+8v, 28 ma av., 36 ma max.
Dissipation:	1.07 watts max.



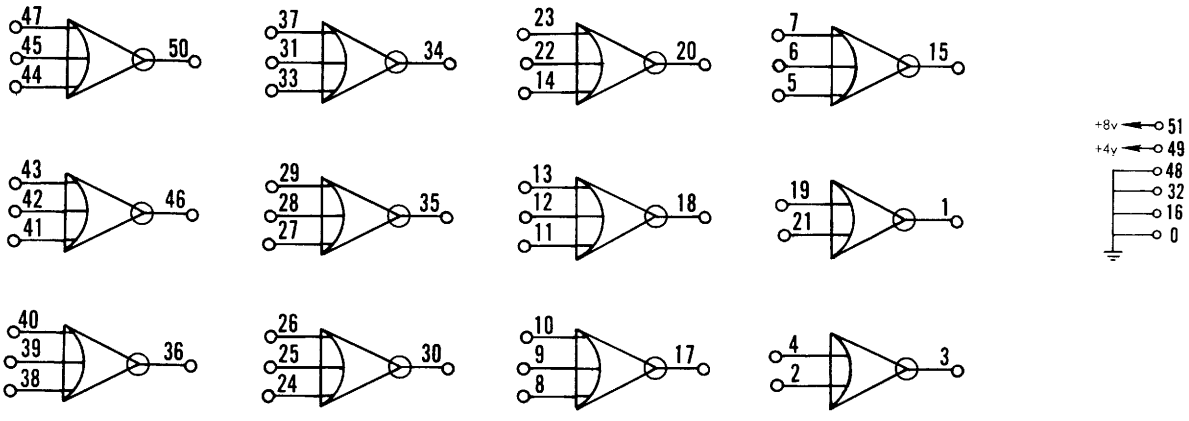
LOGIC DIAGRAM, IT18

INVERTED OR GATES (NOR GATES)

IT27

The IT27 module contains ten 3-input NOR gates and two 2-input NOR gates which have input and output pin numbers identical to those of the BT27. Each circuit can drive 14 unit loads. Various methods are available to expand a NOR gate, by tying outputs together or by adding a second level of gating.

Power Requirements:	+4v, 131 ma av., 234 ma max.
	+8v, 95 ma av., 122 ma max.
Dissipation:	2.1 watts max.



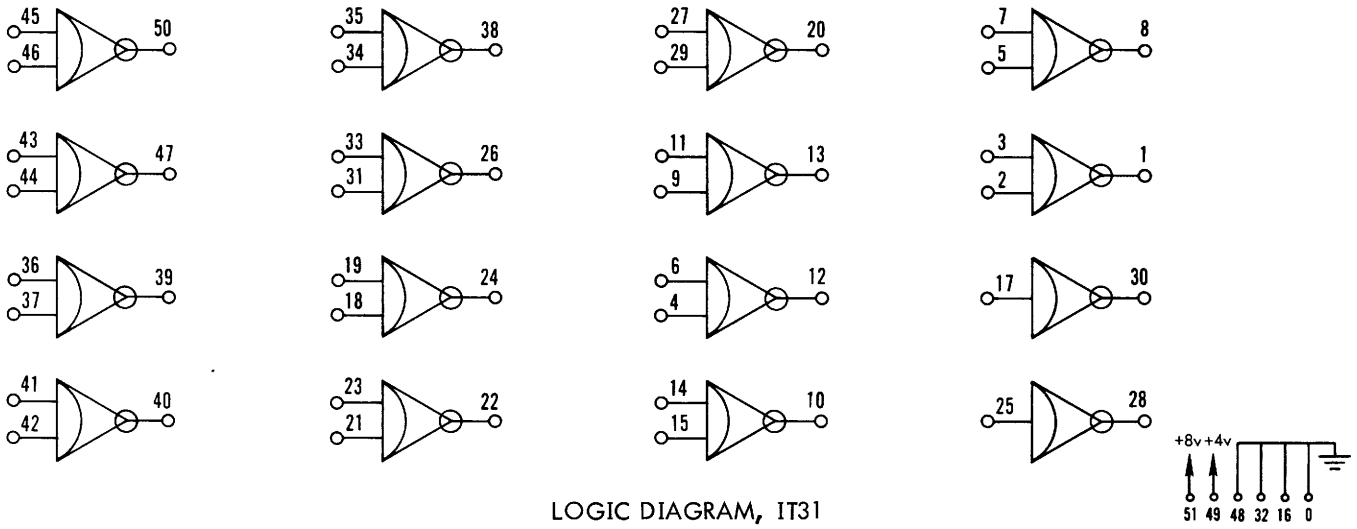
LOGIC DIAGRAM, IT27

IT31

INVERTED AND GATES (NAND GATES)

This module contains fourteen economical 2-input NAND gates and two 1-input inverters intended for general purpose use. Each circuit can drive fourteen unit loads. Gates can be expanded by paralleling outputs with the usual fan-out restrictions. The BT31 module has identical gating but outputs are not inverted (see BT31).

Power Requirements:	+4v, 167 ma av., 312 ma max. +8v, 45 ma av., 57.5 ma max.
Dissipation:	1.88 watts max.



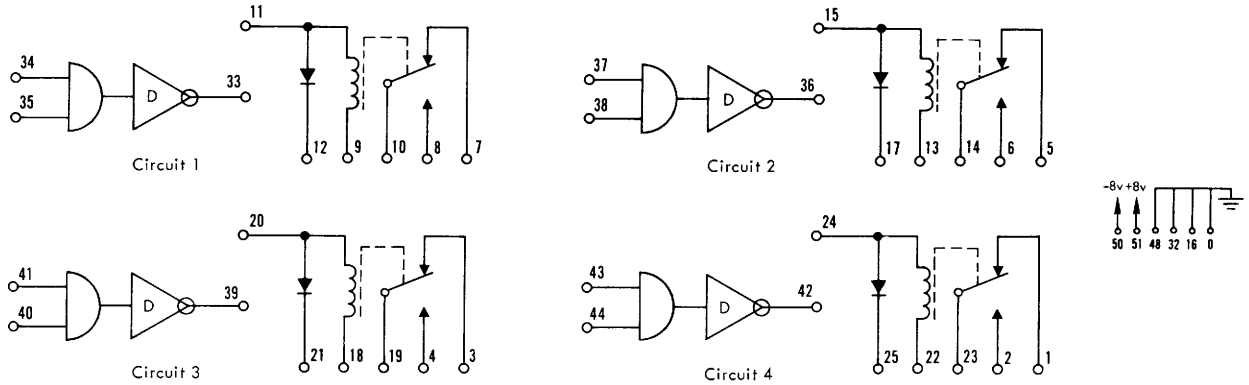
LOGIC DIAGRAM, IT31

KT10

MERCURY-WETTED RELAYS

The KT10 contains four independent relays with mercury-wetted Form C (non-bridging) SPDT contacts. Each relay can be driven by its own 2-input NAND-gate/driver, furnished on the module. A clamping diode limits peak inverse voltage. The relays are single-sided stable. The module occupies two spaces, and must be operated in the prescribed position.

Max. operating frequency:	200 Hz
Circuit delays:	5 millisec. max. make, 1.8 millisec. max. break
Relay coil supply(ea. relay):	30 ma at +6v to 60 ma at +12v
Contact rating:	100 VA max., 500 v max., 2 amp max.
NAND input load (ea. input):	6 unit loads (23 ma) at 0v logic level
Power requirements:	+8v, 63 ma av., 81 ma max. -8v, 2.35 ma av., 5.22 ma max
Dissipation:	0.76 watts plus relay power



LOGIC DIAGRAM, KT10

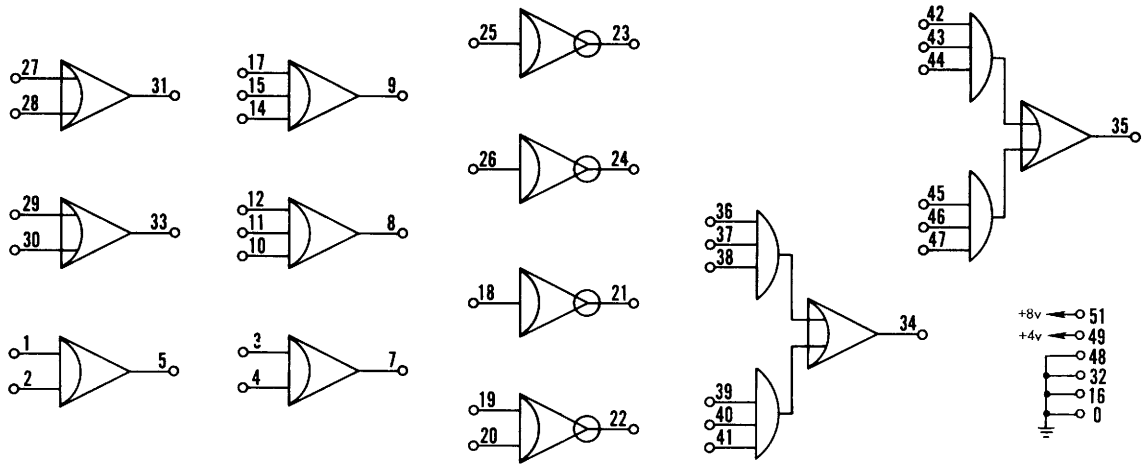
LOGIC ELEMENTS

LT10

LT10 holds several general purpose elements in a useful assortment. The mixture includes 2 Buffered AND/OR gates in which each AND gate has 3 input terms; two 2-input Buffered OR gates; two 3-input Buffered AND gates; two 2-input Buffered AND gates; one 2-input NAND gate and 3 inverters. Each input represents one unit load, and each output can drive 14 unit loads.

Power Requirements: +4v, 138 ma av., 234 ma max.
+8v, 44.8 ma av., 57.5 ma max.

Dissipation: 1.54 watts max.



LOGIC DIAGRAM, LT10

LOGIC ELEMENTS

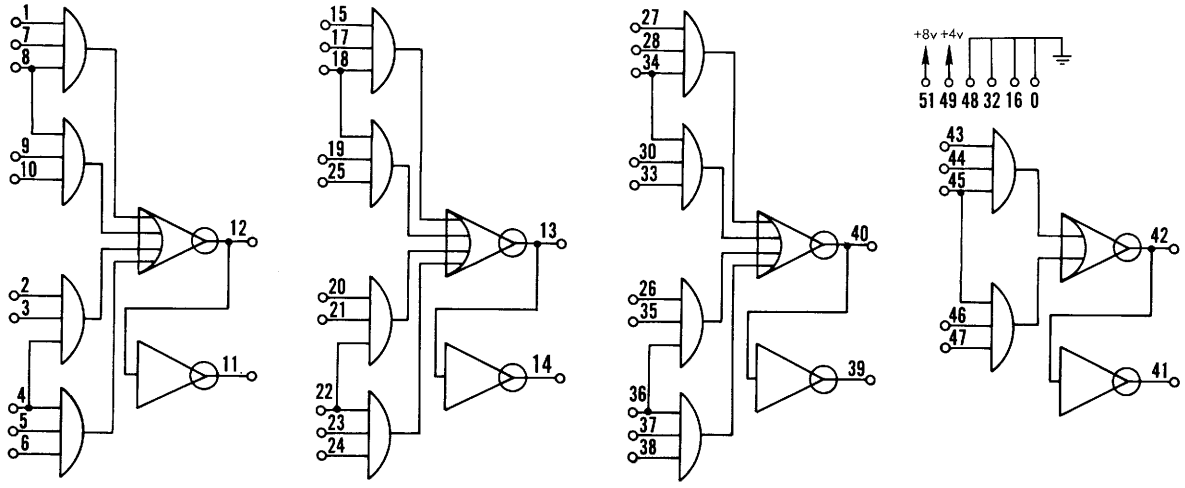
LT11

LT11 has four sets of gates arranged in an AND/OR form, especially suited for selecting sets of bits (in four bit "bytes"), and for forming parallel adders or subtractors, comparators, parity bit generators, and parity bit error detectors as well as many others. Each output has both True and False outputs available. One module can form a parity bit from an 8-bit parallel input, or detect a parity error from 8-bit inputs, or can compare the equality of two 7-bit words.

Fan-outs: 14 unit loads on pins 11, 14 39, 41; 13 unit loads on pins 12, 13, 40, 42.

Power Requirements: +4v, 87 ma av., 148 ma max.
+8v, 50.4 ma av., 64.5 ma max.

Dissipation: 1.22 watts max.



LOGIC DIAGRAM, LT11

LT26

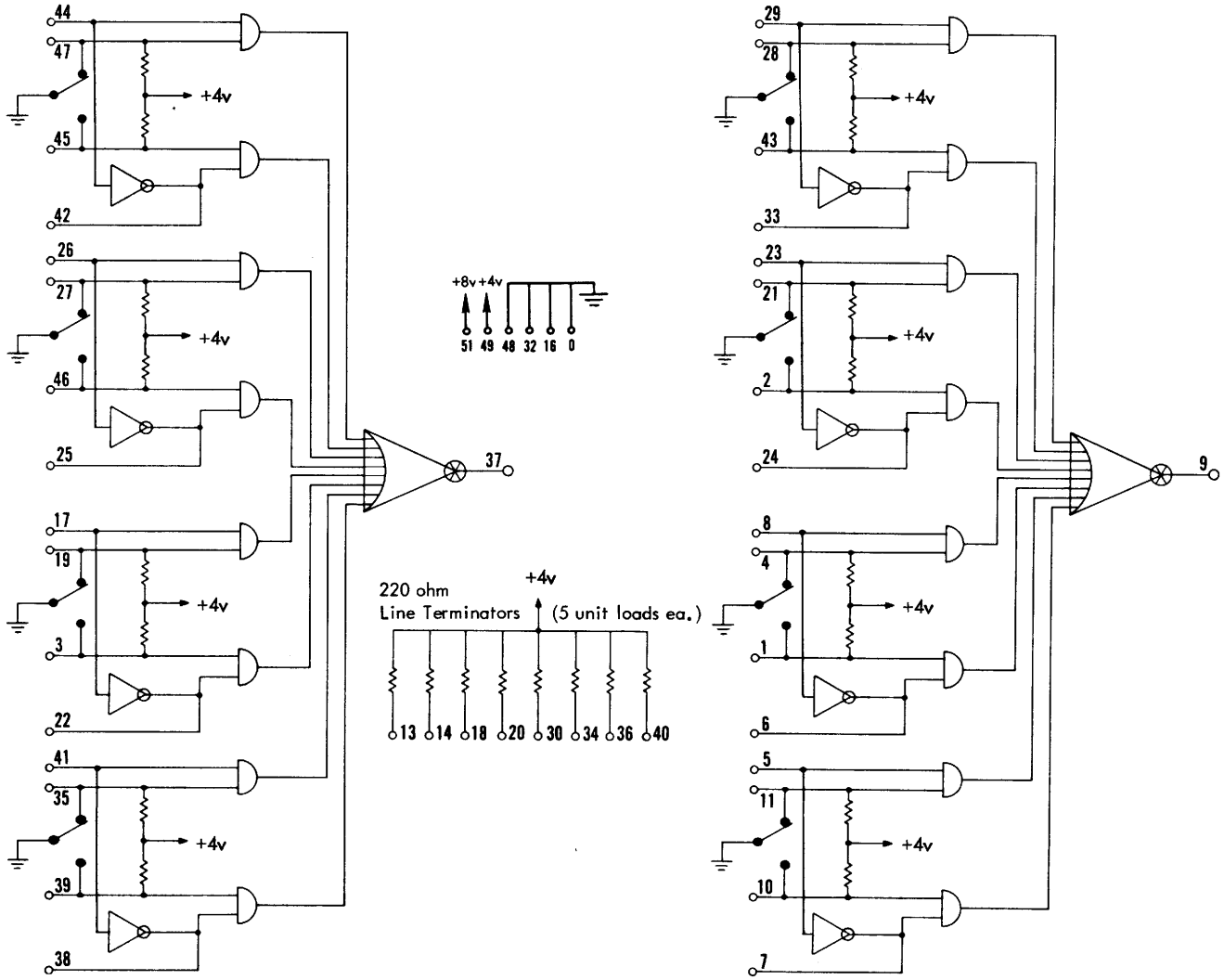
SWITCH COMPARATORS

The LT26 module contains eight switch comparator gates, NORed together in two sets of four. A switch comparator compares the logical state of a signal with the state of a manual toggle switch. When the incoming binary pattern equals the pattern stored in the switches the output of the NOR gate goes True. With the two NOR outputs tied together, an eight bit number can be detected.

Note that a 220 ohm terminating resistor (or 560 ohm pull-up) must be connected to each independent NOR gate output since no 560 ohm pull-up is present on either output. Usually both NOR outputs can be connected to the same 220 ohm resistor, and other buffer or inverter outputs can be connected to the same point to form more complex wired logic functions. Additional terminators are available on the module for conveniently terminating logic lines in accordance with the T Series backpanel wiring rules. A 220 ohm resistor absorbs 5 unit loads.

The eight inverters on the card can also be used independently.

Fan-out (each output):	16-unit loads without pullup or terminator
Power Requirements:	+4v, 171.6 ma av., 324 ma max. +8v, 67.2 ma av., 86.2 ma max.
Dissipation:	2.18 watts max.



LOGIC DIAGRAM, LT26

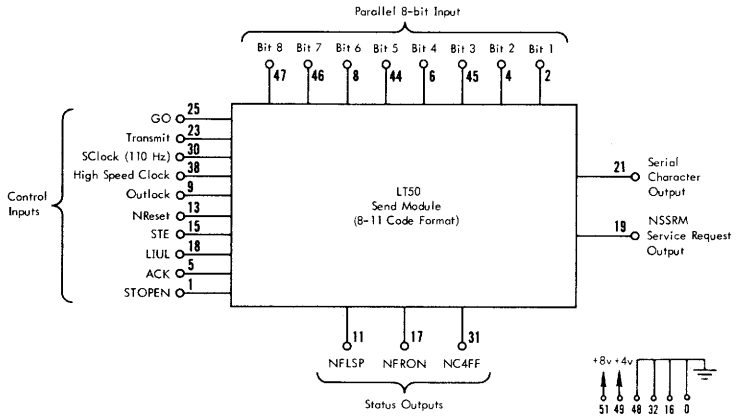
TELETYPE SEND MODULE (8-11 CODE)

LT50

The LT50 is a special purpose logic module which performs a timed parallel-to-serial conversion. It accepts one 8-bit character (8 bits in parallel) and serially transmits the character, together with start and stop signals, to a keyboard-printer (such as a Teletype). LT50 contains an 8-bit shift register, a 5-bit control counter, 3 control flip-flops and other control logic, all on one compact circuit card. Operating speed is determined by the input rate of the keyboard-printer or other character-oriented terminal device. The LT50 performs no code conversion.

Complete design data is given in Application Bulletin 64-51-09. The LT50 can be combined with LT54, NT19, OT14, CT16, and FT12 modules to form an economical character-oriented keyboard-printer interface.

Power requirements:	+4v, 650 ma; +8v, 400 ma
Dissipation:	5.8 watts max.



LOGIC DIAGRAM, LT50

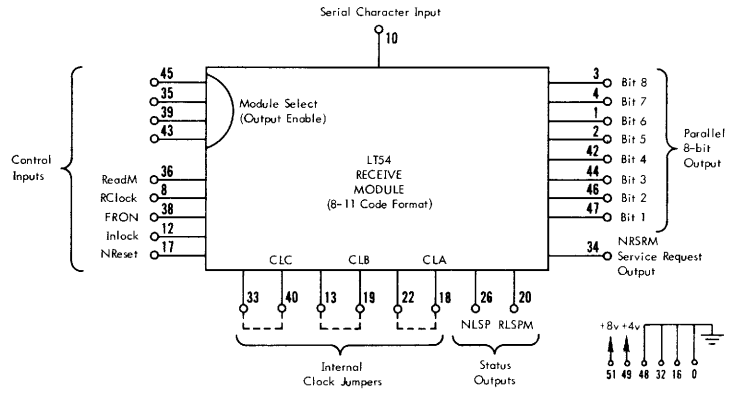
TELETYPE RECEIVE MODULE (8-11 CODE)

LT54

The LT54 is a special purpose logic module which performs a timed serial-to-parallel conversion. It accepts one 8-bit serial character at a time, together with start and stop pulses. It places the eight data bits in a register, for parallel output. LT54 contains an 8-bit shift register, a clock down-counter, 4 control flip-flops and other control logic, all on one compact circuit card. Operating speed is determined by the output rate of the keyboard-printer or other character-oriented terminal device. The LT54 performs no code conversion.

Complete design data is given in Application Bulletin 64-51-09. The LT54 can be combined with LT50, NT19, OT14, CT16, and FT12 modules to form an economical character-oriented keyboard-printer interface.

Power requirements:	+4v, 650 ma; +8v, 400 ma
Dissipation:	5.8 watts max.



LOGIC DIAGRAM, LT54

LT66

12-BIT COMPARATOR

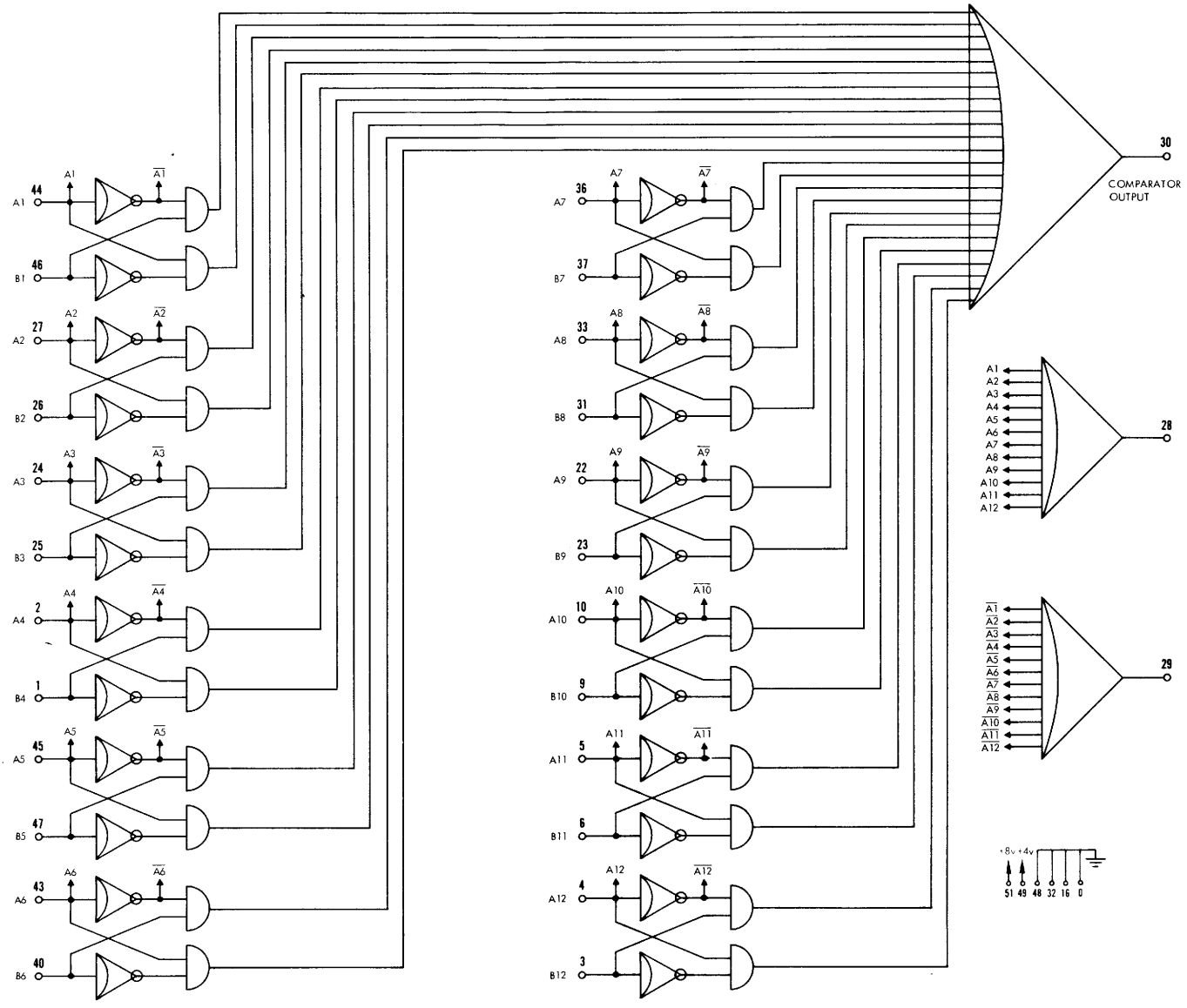
The LT66 contains an array of exclusive-OR logic circuits connected as a comparator. The comparator determines the equality of two twelve-bit words. It compares the two groups designated A and B in the diagram below. The comparator output is False when the two 12-bit patterns are congruent, or True when any two corresponding bits are not equal. The comparator circuit thus solves the equation:

$$Q = \overline{A1}\ B1 + \overline{B1}\ A1 + \overline{A2}\ B2 + \overline{B2}\ A2 + \overline{A3}\ B3 + \overline{B3}\ A3 + \ldots$$

To compare two words, of the same length but less than 12-bits, merely leave unused input pairs open.

The module also contains two 12-bit buffered ANDs. One of these two outputs is True when the group A bits are all True. The other output is True when the group A bits are all False.

Power requirements:	+4v, 224 ma av., 358.5 ma max.
	+8v, 140 ma av., 180 ma max.
Dissipation:	3.06 watts max.



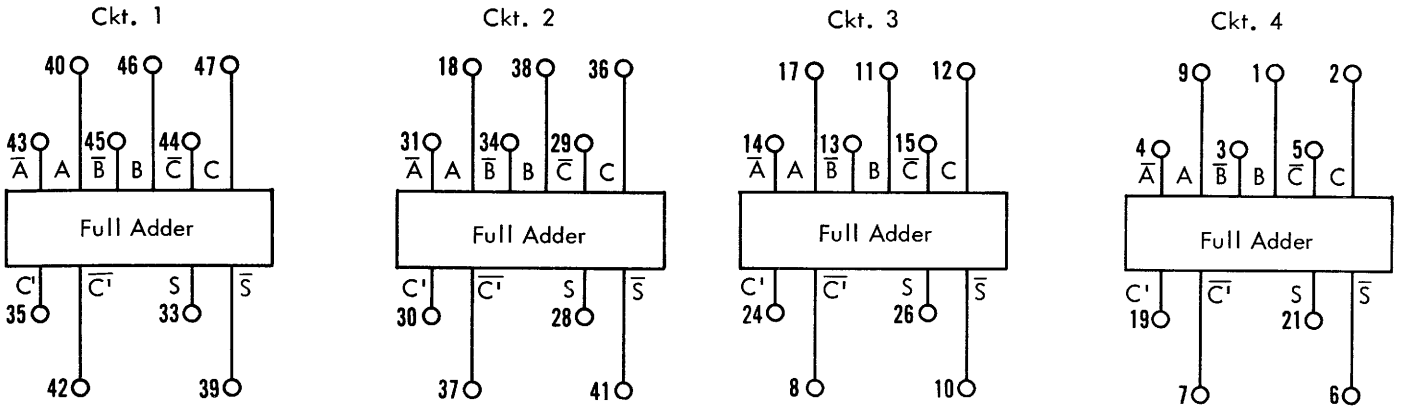
LOGIC DIAGRAM, LT66

FAST FULL-ADDERS

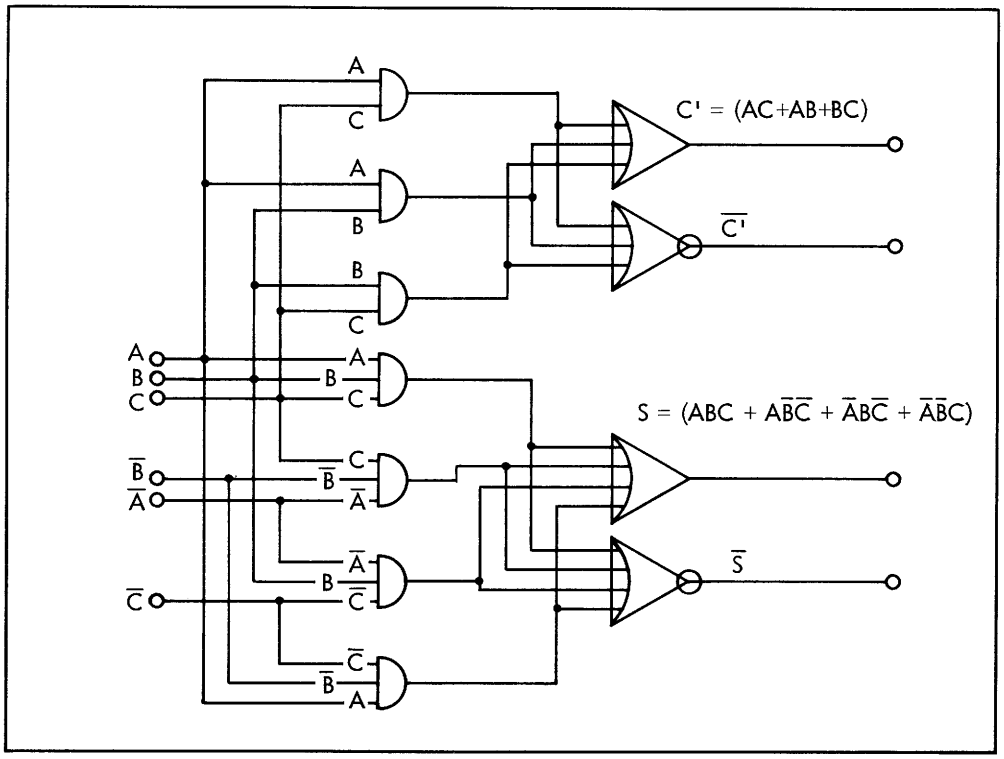
LT67

The LT67 module contains four independent fast-full adder circuits. Each is capable of adding two bits plus carry from a previous stage, and producing sum, carry; sum, and carry outputs. This circuit is a fast adder because only one buffer/inverter delay time (18 nsec typical) is required to add the three input bits and provide output. Most other adder designs require at least two layers of buffers or inverters in series, with consequent longer delay.

Maximum Operating Frequency:	10 Mhz, for 3 stages in series
Circuit delay (per stage):	18 nsec typ., 30 nsec max.
Fan-out (each output):	14-unit loads
Load imposed by inputs:	True inputs: 8 unit loads False inputs: 4 unit loads
Power Requirements:	+4v, 78 ma av., 100 ma max. +8v, 182 ma av., 312 ma max.
Dissipation:	2.26 watts max.



LOGIC DIAGRAM, LT67



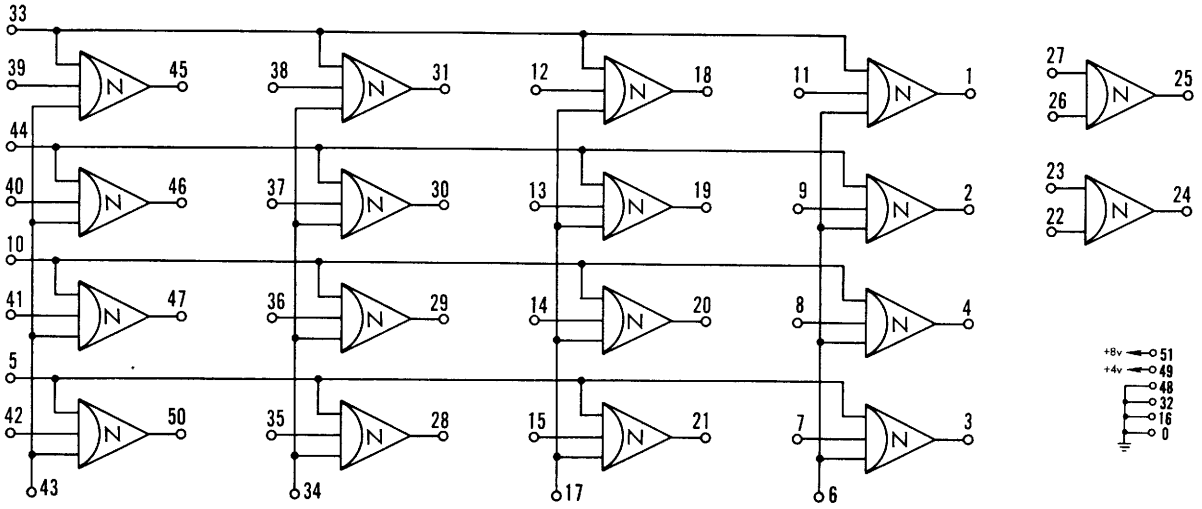
Single Full-adder Circuit (four per module)

NT10

8-VOLT INTERFACE BUFFERS

NT10 contains 2 BANDs and a 4 x 4 matrix of 3-input BANDs. All use standard T Series 0v/+4v input levels. Output levels are 0v and +8v. This module serves as interface from T Series to many other Positive True logic systems which use a high level of about +8v. Input tolerance is often sufficient to permit interfacing with 0v/+6v logic. Standard logic wiring may be used for interfacing provided wire length is under 5 feet. Otherwise use AT14 cable drivers.

Output Current:	53 ma per driver
Power Requirements:	+4v, 132 ma av., 175 ma max.
	+8v, 176 ma
Dissipation:	2.11 watts max.



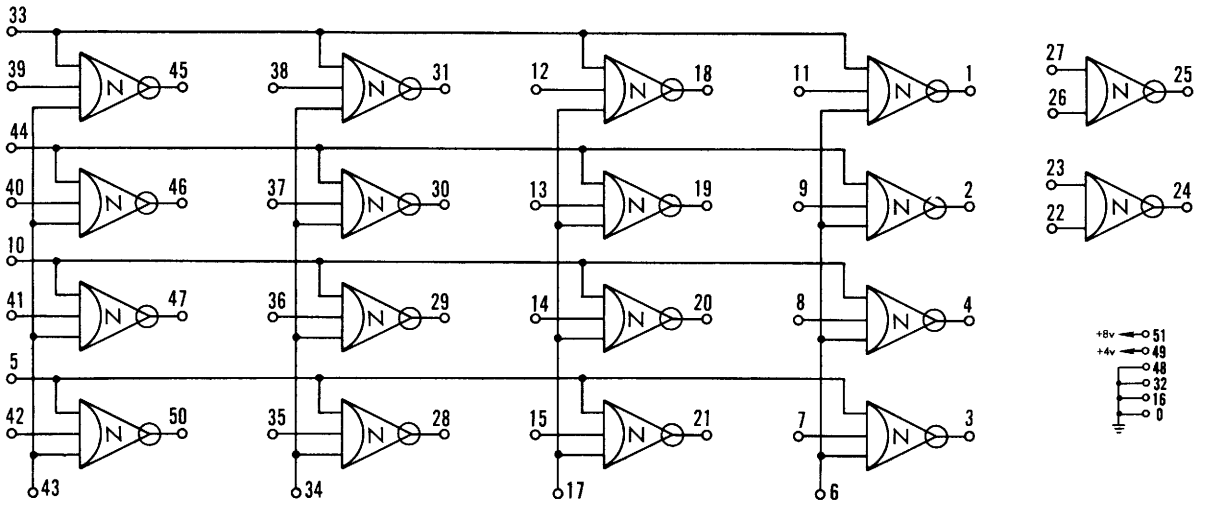
LOGIC DIAGRAM, NT10

NT11

8-VOLT INTERFACE INVERTERS

NT11 contains 2 NANDs and a 4 x 4 matrix of 3-input NANDs. All use standard T Series 0v/+4v input levels. Output levels are 0v and +8v. This module serves as interface from T Series to many other Positive True Logic systems which use a high level of about +8v. Input tolerance is often sufficient to permit interfacing with 0v/+6v logic. Standard logic wiring may be used for interfacing provided wire length is under 5 feet. Otherwise use AT14 cable drivers.

Output Current:	53 ma per driver
Power Requirements:	+4v, 88 ma av., 175 ma max.
	+8v, 176 ma
Dissipation:	2.11 watts max.



LOGIC DIAGRAM, NT11

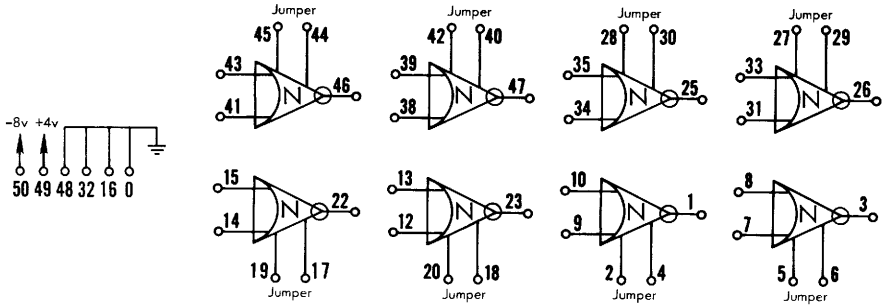
NEGATIVE LOGIC TO T SERIES INTERFACE

NT18

The NT18 contains eight 2-input AND gates which accept 0v/-v input and convert to standard T Series 0v/+4v output.

Maximum negative input voltage is -12 volts. Either of two switching values may be used, as determined by a jumper wire: -1.5v or -3v. When input logic level exceeds -4.5v, the -3v switching value should be used.

Input Current:	-3v to -12v, 4 ma
Power Requirements:	+4v, 120 ma av., 130 ma max.
	-8v, 65 ma av., 100 ma max.
Dissipation:	1.0 watts av., 1.3 watts max.



Note: Add jumper wire to obtain -1.5v switching point.

LOGIC DIAGRAM, NT18

Electrical Truth Table

Input A	Input B	Output
0v	0v	0v
0v	-v	0v
-v	0v	0v
-v	-v	+4v

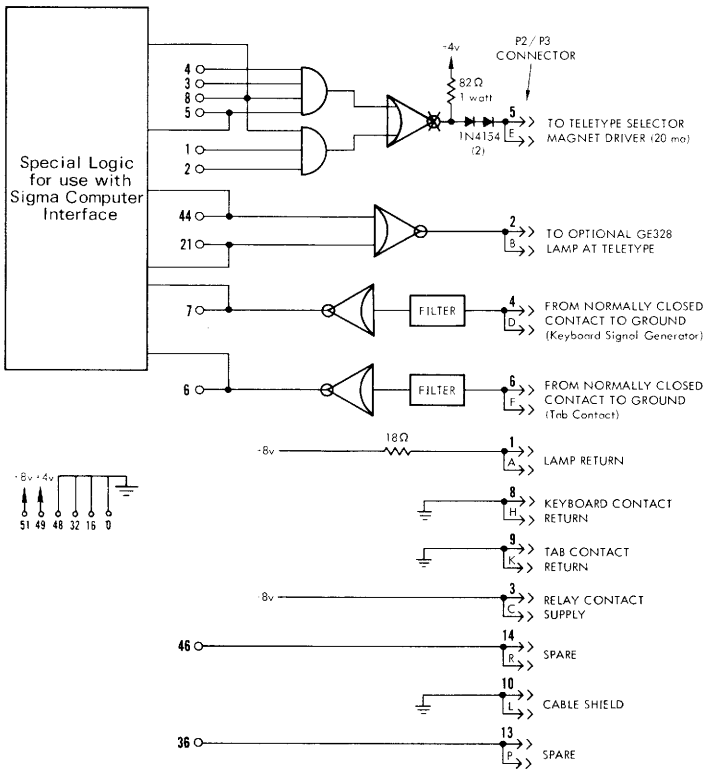
KEYBOARD INTERFACE

NT19

The NT19 is a special purpose module meant to provide a proper electrical match between T Series logic (LT50 and LT54 modules) and a keyboard-printer (such as a Teletype), using 500 feet or less of ET12 cable. In addition the NT19 contains special logic required when the module is used as part of a Sigma 2 Computer. The presence of the special logic, when not used, affects only the loading of some inputs and outputs.

For complete design data refer to Application Bulletin 64-51-09, which describes an economical character-oriented data interface unit.

Power requirements:	+4v, 64 ma; +8v, 325 ma
Dissipation:	2.86 watts max.



LOGIC DIAGRAM, NT19

NT33

T SERIES TO NEGATIVE LOGIC INTERFACE

The NT33 module contains eight 2-input gates which accept standard T Series logic levels as input and furnish 0v and -v logic levels as output. A negative voltage as low as -30 volts can be used as a negative logic level. It must be supplied from an external source and wired to pin 17.

The NT33 is similar to the discontinued model NT17. The important differences between the two modules are:

1. The NT33 will accept -v down to -30 volts; the NT17 will accept -12 volts.
2. NT33 max. output sinking current is 140 ma over its output voltage range; max. NT17 current is 20 ma.
3. NT33 rise and fall times are controlled with a capacitor (C4).
4. NT33 provides a high output impedance to the line (>200K ohms) when power is off.

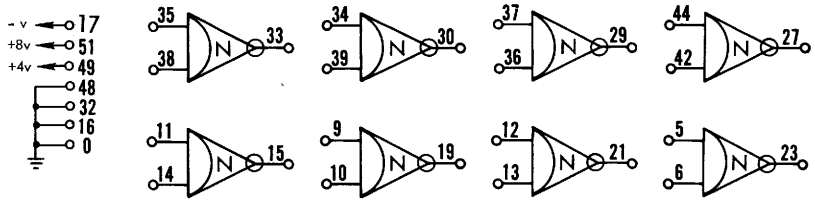
The NT33 provides an excellent match with Univac and CDC equipment, meeting all specifications. NT33 can be paired with AT69.

Other variations to NT33 output impedance and rise/fall time can be made on special order.

Switching threshold:	2.0 volts typ.
Output current (sinking) (from -3v to -30v):	140 ma max.
Propagation delay, to 90% of -v (at no load):	500 ns max.
+4 volt supply (Vcc):	ma 48** 56**
+8 volt supply:	ma 20** 25**
-8 volt supply:	ma 70** 80**
-v supply:	ma depends on -v supply voltage
Dissipation, per module (using example of -20v):	watts: 2.02** 2.39**

* Maximum data rate depends on value of rise time control capacitor (C4) and length of cable driven. Data rates range from 100 Khz to better than 1 Mhz.

** At 50% duty cycle.



Electrical Truth Table

Input 1	Input 2	Output
0v	0v	0v
+4v	0v	0v
0v	+4v	0v
+4v	+4v	-v

OT14

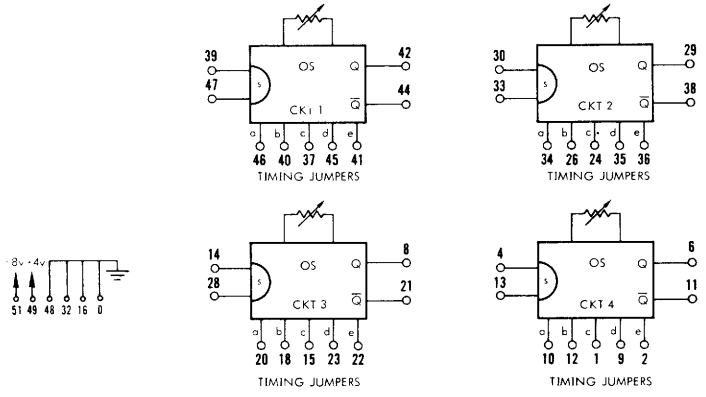
ADJUSTABLE ONE-SHOTS (MEDIUM DELAY)

OT14 contains four one-shots having output pulsewidth adjustable from 50 μsec to 2.2 sec. Minimum input enable time is 30 nsec True. Q output goes True within 75 nsec or less after enabling trailing edge reaches +2v. Do not retrigger during recovery time.

Delay is determined by connecting internal capacitors with jumpers (Table 1) and adjusting pot within the range obtained.

Pulsewidth range:	50μsec to 2.2 sec.
Pulsewidth tolerance:	±10%
Fan-out:	14 unit loads/Q output 12 unit loads/$\overline{Q}$ output
Power requirements:	+4v, 185 ma; +8v, 120 ma
Dissipation:	1.7 watts max.

P.W.	CONNECTION
50 - 350 SEC	NONE
0.3 - 3.5 MILLISEC	A - E
3 - 35 MILLISEC	B - E
25 - 300 MILLISEC	C - E
0.2 - 1.5 SEC	D - E
0.3 - 2.2 SEC	C - D - E



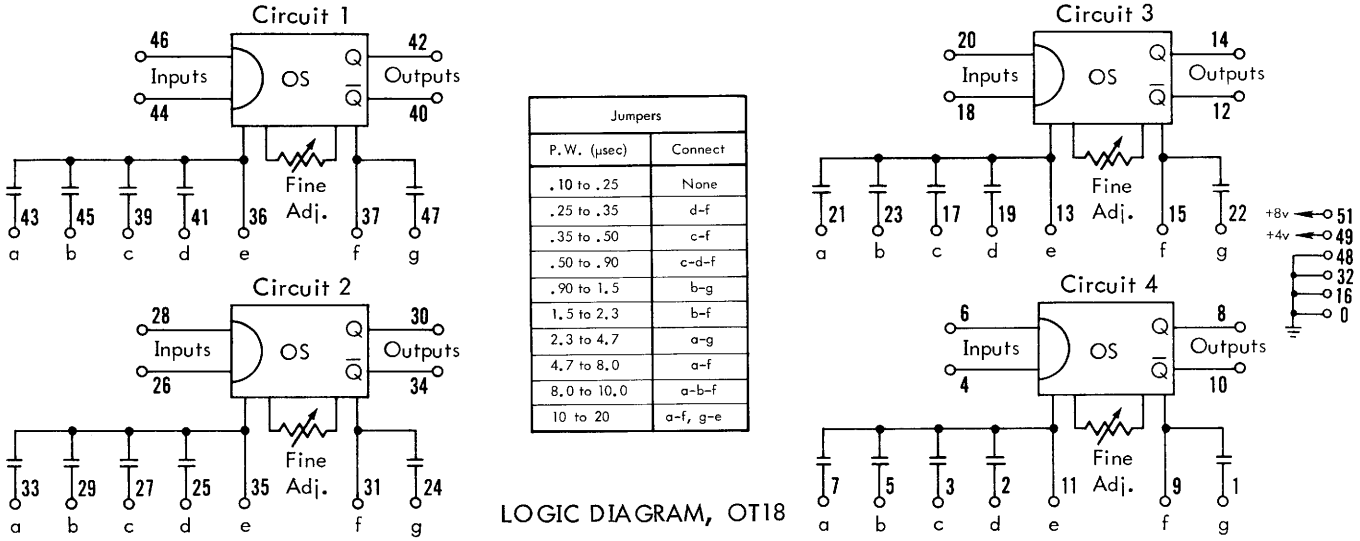
ADJUSTABLE ONE-SHOTS (SHORT DELAY)

OT18

OT18 contains 4 circuits having continuously adjustable pulsewidth of 100 nsec to 20 μsec. Minimum input pulse is 50 nsec True. Leading output edge starts typically 45 nsec after input trailing edge reaches +2 volts. Duty cycle is 50%; circuit may not be retriggered before end of cycle. External capacitance may be placed on the module (standoffs E1, E2) to extend the pulsewidth to 20 milliseconds.

Pulsewidth = 1.3C (C in μf, P. W. in millisec).

Pulsewidth range:	100 nsec to 20 μsec
Pulsewidth tolerance:	±10%
Fan-out:	14 unit loads per output
Power requirements:	+4v, 260 ma
	+8v, 65 ma
Dissipation:	2 watts



Jumpers	
P.W. (μsec)	Connect
.10 to .25	None
.25 to .35	d-f
.35 to .50	c-f
.50 to .90	c-d-f
.90 to 1.5	b-g
1.5 to 2.3	b-f
2.3 to 4.7	a-g
4.7 to 8.0	a-f
8.0 to 10.0	a-b-f
10 to 20	a-f, g-e

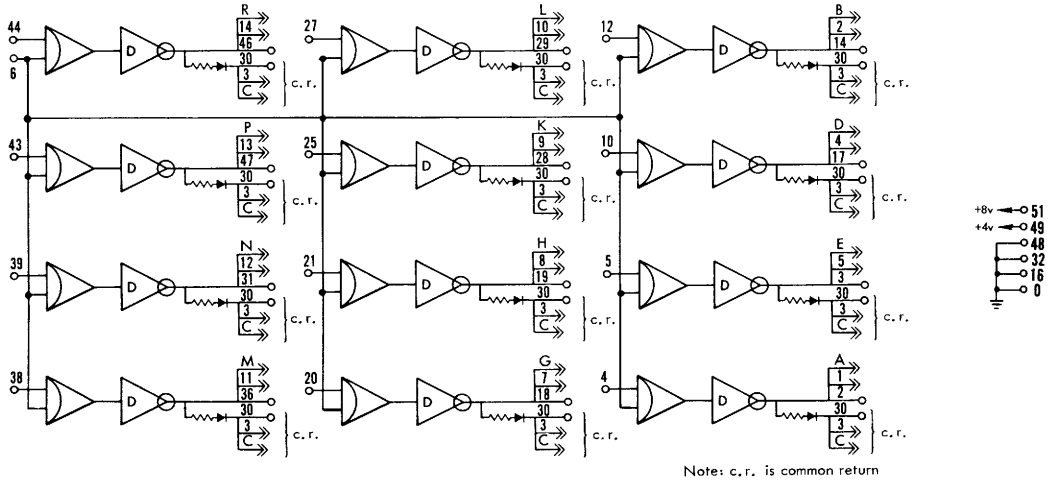
LOGIC DIAGRAM, OT18

LAMP DRIVERS

QT14

The QT14 has 12 circuits, each capable of switching an externally supplied current of 200 ma at voltage up to +28v. Driver outputs go to front-edge contacts on the module for use with ET11 cable connectors. The keep-warm resistors and overload protection diodes connect to common ground. Output rise and fall are slowed to minimize noise. Operating frequency is limited by lamp response. Refer to RT14 for similar circuit.

Power Requirements:	+4v, 268 ma av., 535 ma max.
	+8v, 41 ma
Dissipation:	2.47 watts max.



Note: c.r. is common return

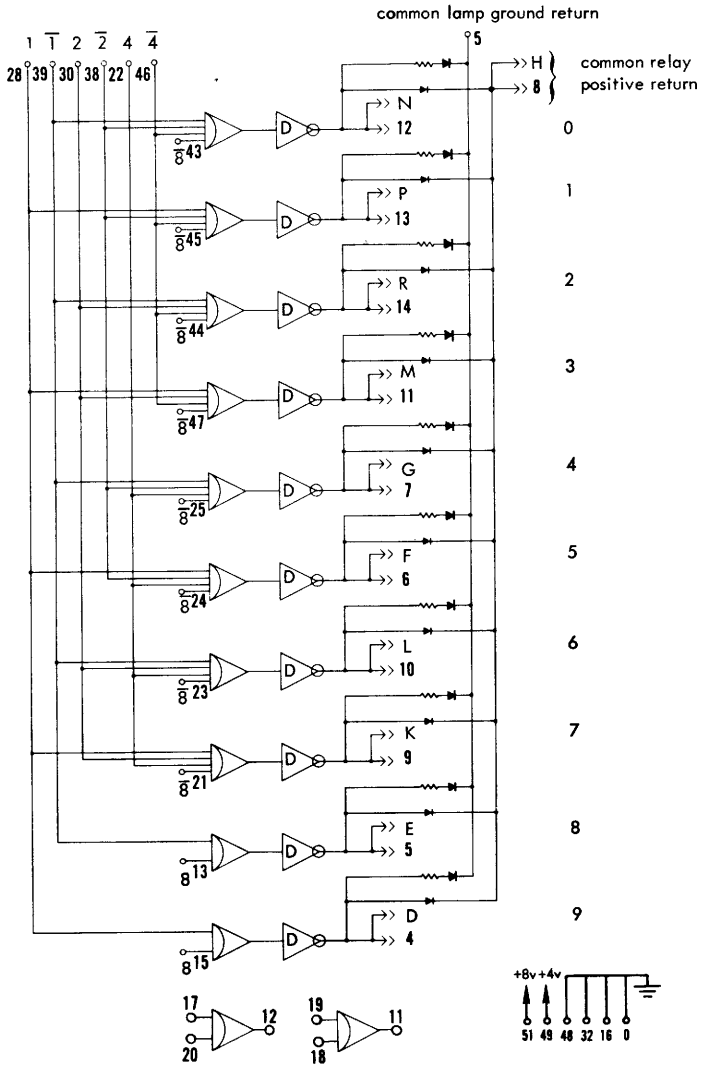
LOGIC DIAGRAM, QT14

QT16

BCD-DECODER/DRIVERS

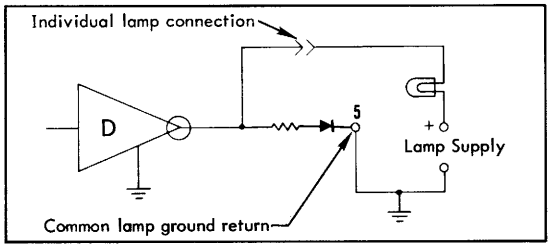
The QT16 module contains ten high-current drivers, suitable for driving lamps or relays. The drivers are controlled by a BCD-to-decimal decoding network; this makes it possible to drive a ten-lamp display directly from any BCD output without the need for intervening gating. Both logic phases, non-inverted and complementary, must be provided. Each AND gate in the decoding network also has an independent AND input which can be used to inhibit the driver, or drive it independently (with all BCD input lines True).

Outputs are supplied to circuit etch contacts at the front edge of the module for connection to cables via a pair of ET11 cable connectors. In addition, back-panel pins, 1, 2, and 3 are connected straight through via etch to corresponding front-edge contacts.

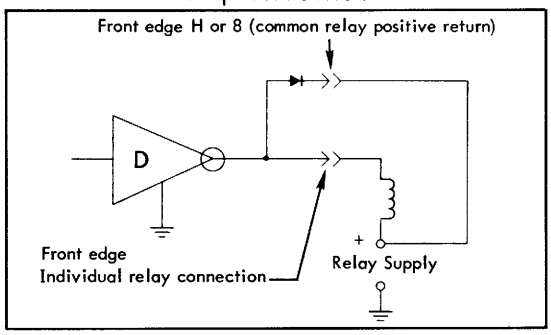


LOGIC DIAGRAM, QT16

Max. operating frequency:	250 Khz
Circuit delay:	0.5 μsec
Output switching capability:	28v max., 200 ma max.
Load imposed by each input term:	4 Unit Loads on pins 30, 38, 22, 46; 5 Unit Loads on pins 28, 39; all others 1 Unit Load
Power Requirements:	+4v, 220 ma av., 369 ma max. +8v, 33.6 ma av., 43.2 ma max.
Dissipation:	2.0 watts max.



Lamp Connection



Relay Connection

QT17 BCD-DECODER/INDICATORS

QT17 contains 12 white indicator lamps mounted near the front edge of the module. This module is pin-compatible with QT16 and may be used for local checkout of logic prior to installation of that Decoder-Driver Module.

A BCD-to-decimal decoding network controls 10 lamps; each of the other two lamps are preceded by a 2-input AND. All lamps can be operated independently by leaving the decoding network input lines open (True), and controling each lamp using the independent input provided.

This indicator module operates from standard T Series logic level inputs. The lamp turns On when all inputs at its controlling gate are True.

For pin number assignments and basic overall logic arrangement, see QT16 logic diagram.

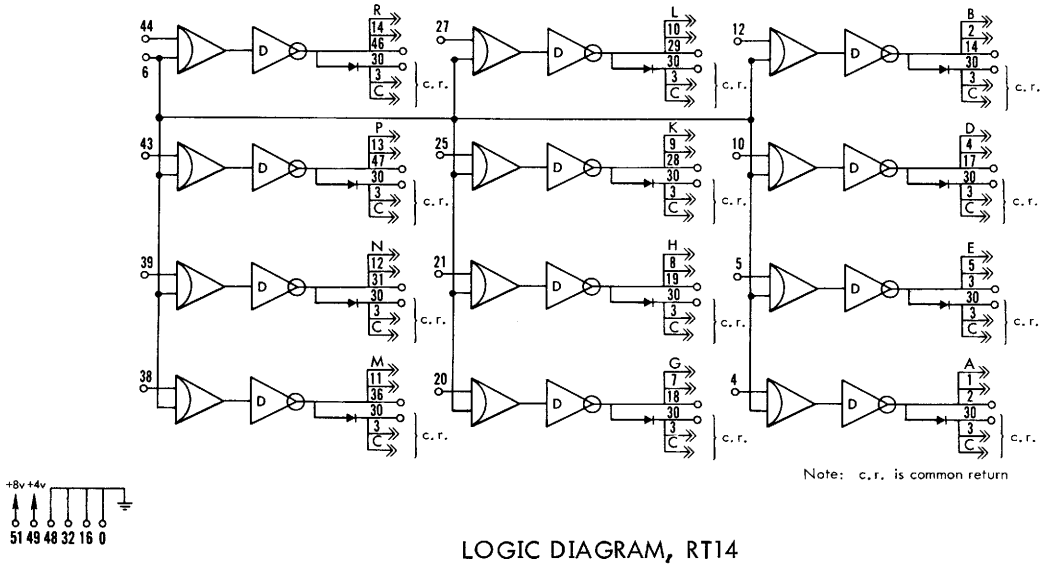
Load imposed by each input term:	4 Unit Loads on pins 30, 38, 22, 46; 5 Unit Loads on pins 28, 39; all others 1 Unit Load.
Power Requirements:	+4v, 404 ma av., 504 ma max., plus 45 ma for each On lamp +8v, 33.6 ma av., 43.2 ma max. 2.6 watts max. w/bulbs off

RELAY DRIVERS

RT14

The RT14 has 12 circuits, each capable of switching an externally supplied current of 200 ma at voltage up to +28v. Driver outputs go to front-edge contacts on the module for use with ET11 cable connectors. The peak inverse voltage protection diodes are connected across the relay coils by connecting common return to +v. Output rise and fall are slowed to minimize noise. Operating frequency is limited by relay response. Refer to QT14 for similar circuit.

Power Requirements:	+4v, 268 ma av., 535 ma max.
	+8v, 40.8 ma.
Dissipation:	2.47 watts max.



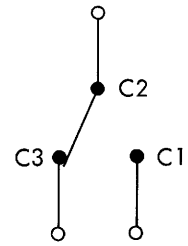
LOGIC DIAGRAM, RT14

MANUAL TOGGLE SWITCHES

ST14

The ST14 module has fifteen SPDT toggle switches for manually setting logic levels into gating circuits, or other use. Contacts are rated for 5 amp. at 115v. In the diagram below, switch is shown in the "1" position of the handle .

Pin Connections											
Ckt.	C2	C3	C1	Ckt.	C2	C3	C1	Ckt.	C2	C3	C1
1	46	45	47	6	43	42	44	11	39	38	40
2	34	29	35	7	37	36	41	12	31	30	33
3	21	20	22	8	27	26	28	13	24	23	25
4	11	7	12	9	14	13	19	14	17	15	18
5	2	1	3	10	5	4	6	15	9	8	10

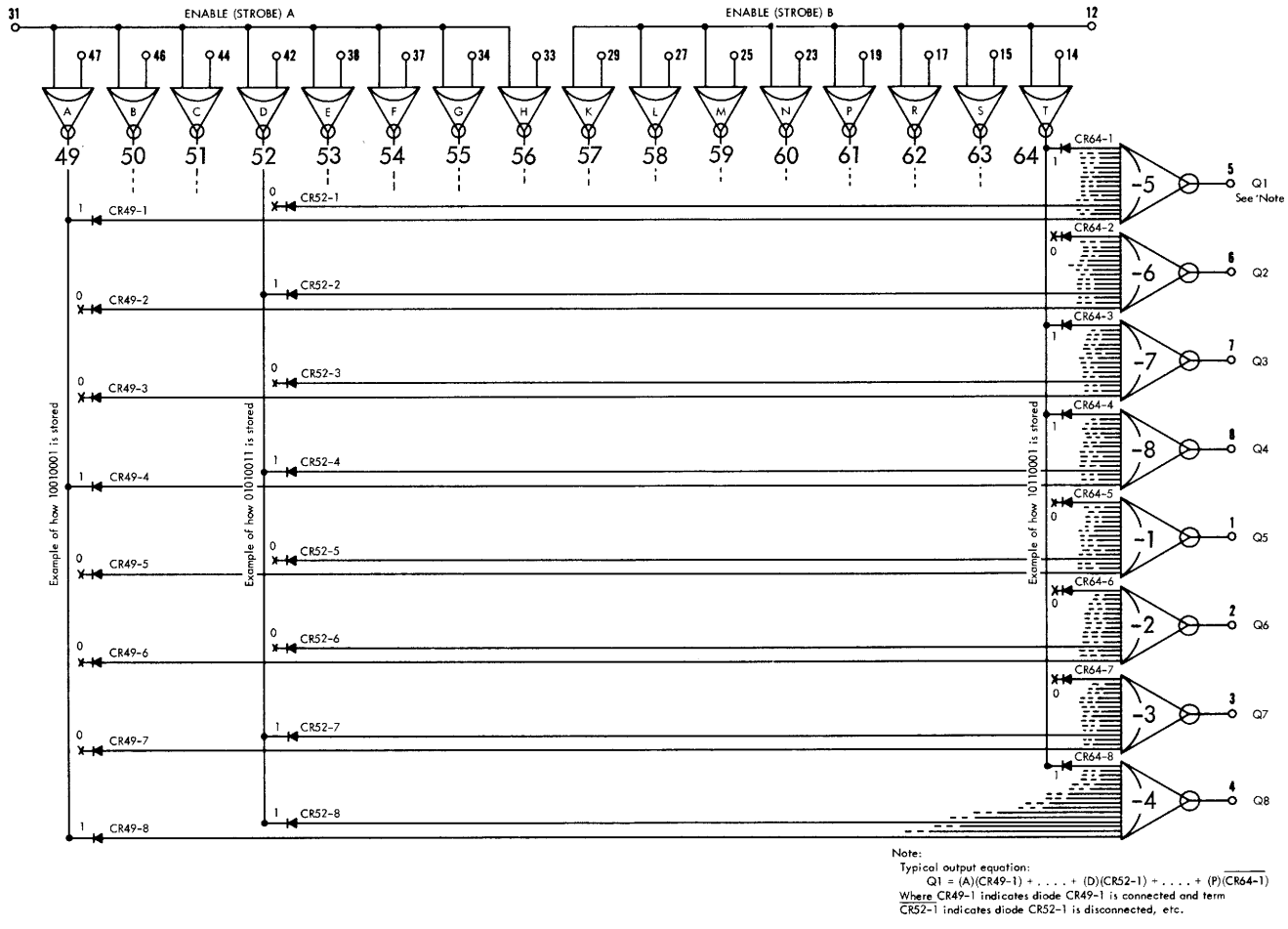


The ST44 stores sixteen 8-bit bytes in a diode matrix. When one of sixteen input lines is energized (together with its strobe line) an 8-bit pattern appears at the outputs. The 8-bit pattern that results from a given input is always the same, and is determined by the pattern of diodes connected between the input line and the output lines. Presence of a diode between an input line and a particular output line produces a 1 in the particular output whenever the input goes True; absence produces a 0 (see examples on logic diagram).

The ST44 acts as a memory: when one address (one of sixteen input lines) is made True, a predetermined 8-bit byte appears at the output. Outputs are normally 0 (low) when input is 0 (low). Each ST44 module is supplied with a diode in place at every crossover, initially providing a memory whose output is all 1's. Zeros are entered where desired by clipping out diodes with a wire cutter (shown in the example below by the diagram ✕◀——---).

If two input lines are raised simultaneously, then each output line will contain the logical OR of the bit-pairs which were energized. For example, if input 1 normally provides 10010001 and input 2 normally provides 01010011, then the output will be 11010011 when both input 1 and input 2 are raised together.

Input 1		Input 2		Output
1	+	0	=	1
0	+	1	=	1
0	+	0	=	0
1	+	1	=	1
0	+	0	=	0
0	+	0	=	0
0	+	1	=	1
1	+	1	=	1



LOGIC DIAGRAM, ST44

The ORing characteristic makes it possible to store more than sixteen 8-bit bytes per module, providing that more than one input is raised at once, and providing the resulting pattern is not already present on the module.

A 4-bit binary addressing control for the sixteen input lines can be created with a BT12 module, which accepts a 4-bit input and decodes in straight binary fashion to 1-of-16 outputs. Input to the BT12 can be derived from a 4-bit counter. Thus, the combination of 4-bit counter, BT12 decoder, and ST44 memory creates an economical 16 word program control.

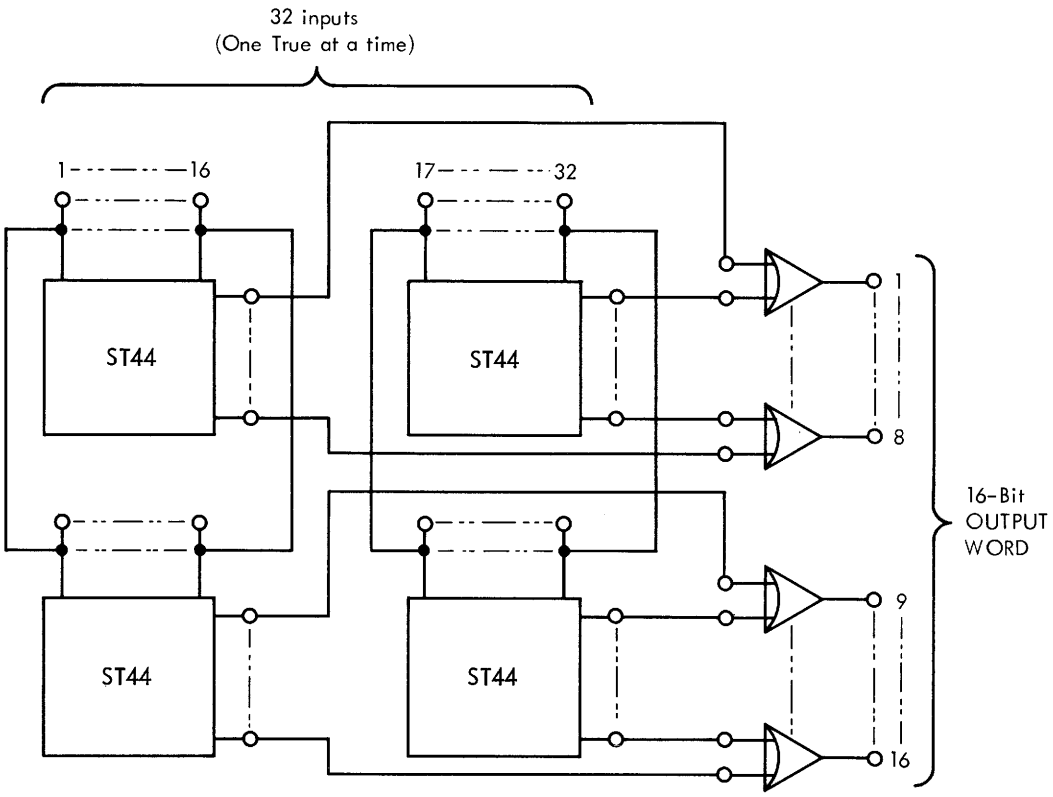
Word length can be expanded in increments of 8-bits by paralleling the input lines of additional ST44 modules. Each time an input on one ST44 is raised, resulting in 8-bits of output, a corresponding input on another ST44 is also raised, resulting in 8 more bits of output.

The number of words stored can also be expanded, by ORing outputs of additional ST44 modules to maintain the same number of output buses.

An example of how these two techniques can be combined to create a read only memory containing thirty-two 16-bit words is shown in the diagram below.

Maximum operating frequency:	10 MHz
Circuit delay:	50 nsec maximum
Input loading:	1 unit load/input
	8 unit loads/enable (strobe)
Power requirements:	+4v, 262 ma av., 468 ma max.
	+8v, 67.2 ma av., 86.2 ma max
Module dissipation:	2.8 watts max.

* This module is also available with diodes not inserted. A package of 100 loose diodes is included. The user programs the module by inserting diodes instead of removing them. Request Model ST41.



Expansion to thirty-two 16-bit Words (512 bits)

WT49

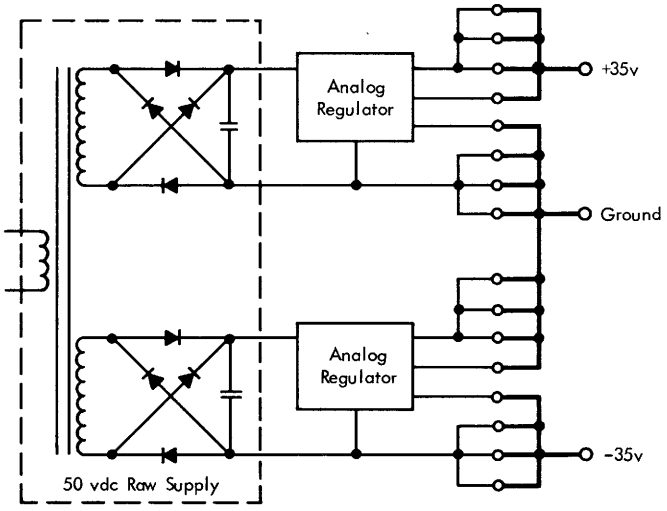
REFERENCE VOLTAGE REGULATOR

The WT49 module contains two electrically independent precision 35 volt regulators. The regulators have remote sensing capability and are short circuit proof for a period of 30 seconds.

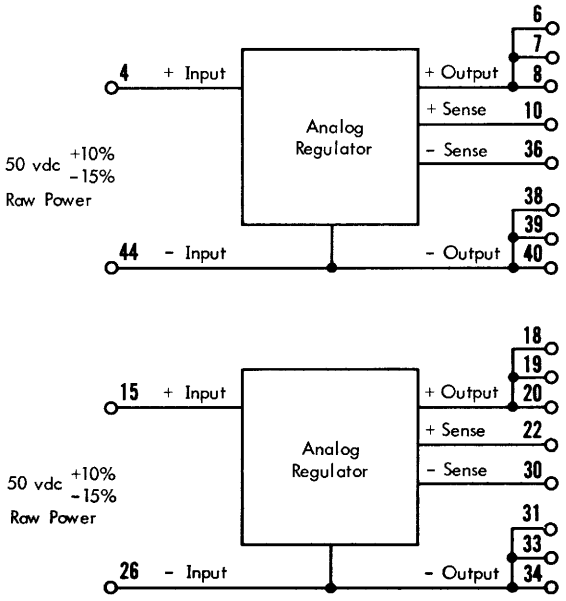
Each of the regulators may be used for either plus or minus polarity, much like a battery, by grounding the appropriate side. One WT49 module can supply both +35v and -35v reference voltages for use with digital-to-analog converter modules such as the DT24. One WT49 module can supply twenty-four DT24 modules.

All pins shown below on one input or output should be bussed together on the connector, or on long runs should be wired in parallel to reduce the current per wire. Where IR drop is expected to be a problem, wire the sense inputs to a representative point in the load. Otherwise wire sense inputs to outputs on the WT49. The WT49 requires one card slot. Because of the high dissipation it is advisable to either leave an empty card slot beside the component side of a WT49, or place a cable-plug or other passive module beside the component side.

Output voltage:	35 vdc, + or -, adjustable to within 3 mv
Output current:	0 to 250 ma., each regulator
Load regulation:	0.03%
Ripple rejection:	400:1 min.
Temperature coefficient:	<0.003%/°C from 0°C to +55°C
Operating temperature range:	0°C to +55°C
Power Requirements: (each regulator)	42 vdc min. to 55 vdc max. at 300 ma max., isolated from ground. May be obtained from PT23 supply.
Module dissipation: (both regulators)	12.5 watts max.



CONNECTION AS ±35 vdc SUPPLY



INPUT-OUTPUT DIAGRAM, WT49

25V REFERENCE VOLTAGE REGULATOR
15V REFERENCE VOLTAGE REGULATOR

WT53
WT54

The WT53 and WT54 each contain two electrically independent precision regulators, which are short circuit proof for a period of 30 seconds. The WT53 delivers ±25 volts, while the WT54 delivers ±15 volts.

Each regulator circuit may be used for either plus or minus polarity, much like a battery, by grounding the appropriate side. Thus one module with its two independent regulator circuits can supply both + and - reference voltages (see connection diagram).

All pins that are shown on one input or output should be bussed together on the backplane connector. On long runs use parallel wires from the regulator to the destination to reduce IR drop.

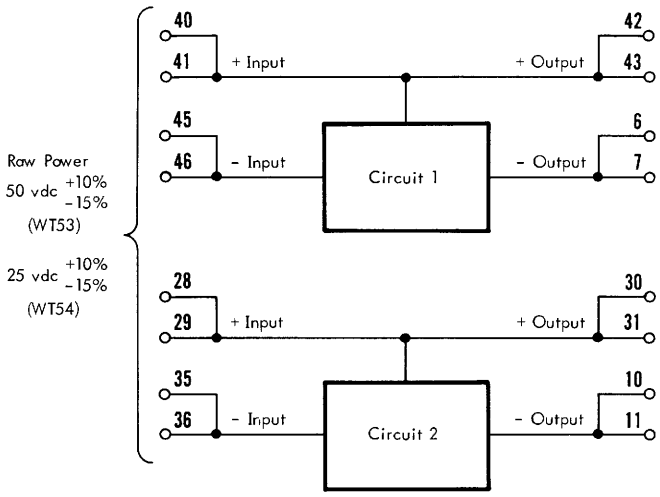
One regulator module requires two card slots. However, because of the high dissipation it is advisable to either leave an empty slot beside the component side, or place a cable-plug or other passive module beside the component side.

Characteristic	Units	Min.	Typ.	Max.
Outputs				
WT53 nominal output voltage†	vdc		25	
WT53 voltage adjust resolution	mv	±40		
WT53 output current, each ckt. (I out)	amp.			0.4
WT54 nominal output voltage†	vdc		15	
WT54 voltage adjust resolution	mv	±20		
WT54 output current, each ckt. (I out)	amp.			1.0
Load regulation	%	1		
Ripple rejection		50:1		
Temperature coefficient (from 0°C to +55°C)	%/°C			0.05
Operating temperature range	°C	0		+55
Inputs				
WT53 input voltage range* (for nominal outputs)	vdc	29	49	55**
WT53 input current	amp.			0.55
WT54 input voltage range* (for nominal output)	vdc	19	22.5	26**
WT54 input current	amp.			1.2
Dissipation, per module	watts			24

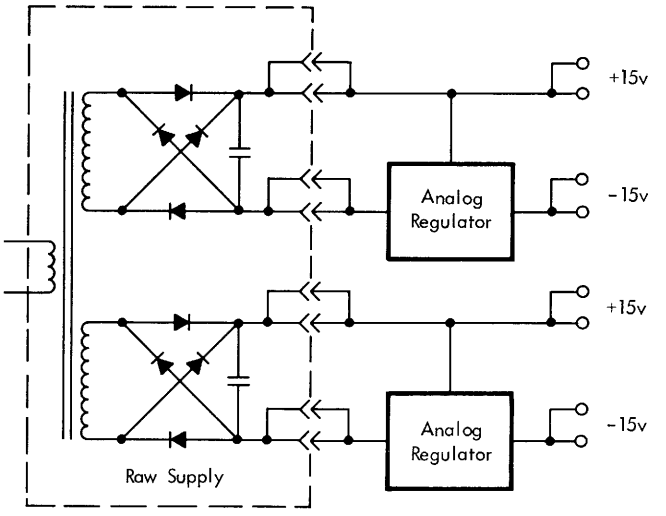
† Output voltage can be adjusted over a range of ±2.5 volts on WT53, and ±2 volts on WT54.

* Isolated from ground. May be obtained from PT23 or PT26 supply.

** Do not use this value of maximum input voltage under maximum current load.



WT54 CONNECTION DIAGRAM



INPUT-OUTPUT DIAGRAM

XT10

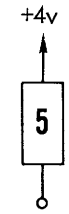
LINE TERMINATORS

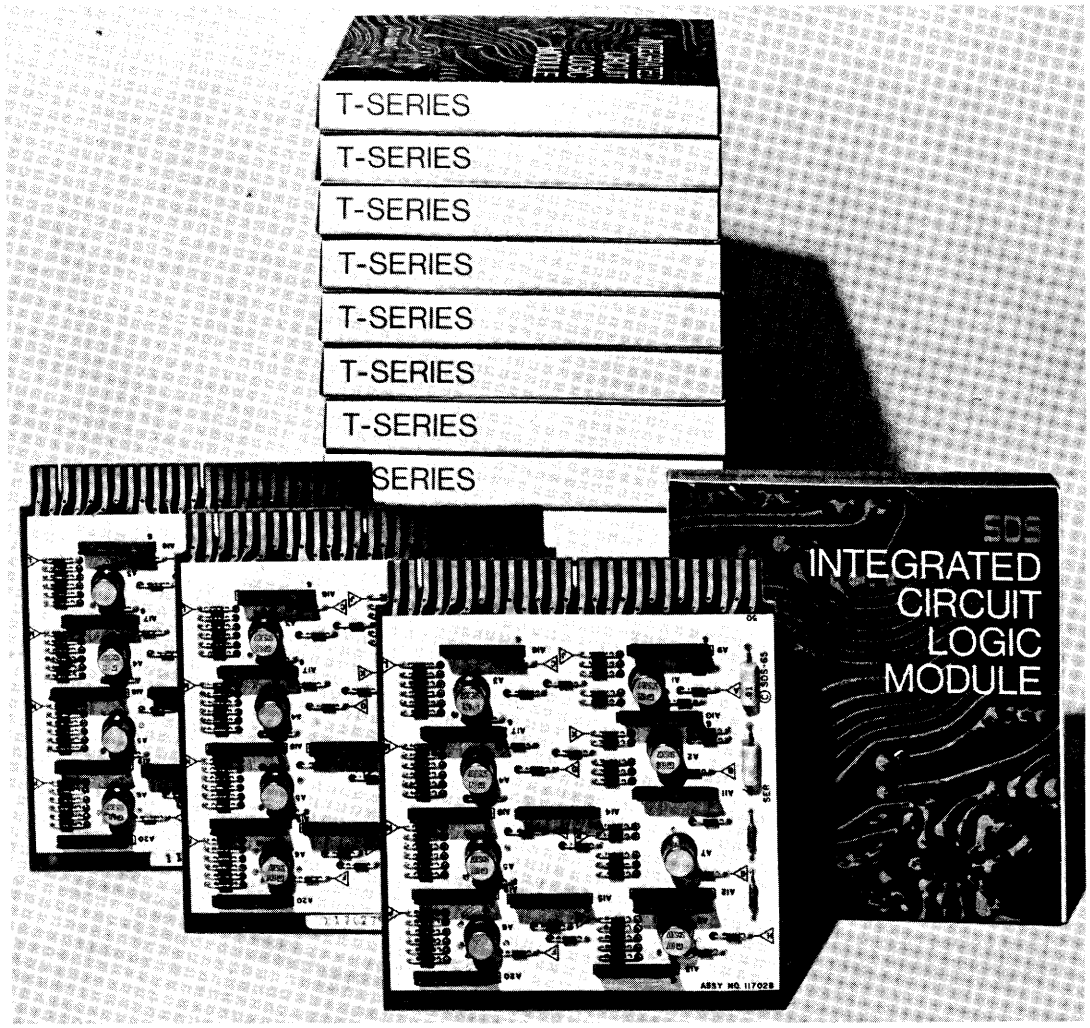
The XT10 module has forty-six 220 ohm resistors returned to +4v. They are used as line terminations for back panel wiring. Each terminator uses 5 unit loads of the driving circuit's fan-out. A maximum of 2 terminators may be used with one driver output, connected to the ends of two driven lines. No more than 1 terminator may be connected to one driven line. The terminators are required to achieve high propagation speeds and minimize signal reflections when logic lines are long. They need not be used when lines are short or when lower propagation speeds are acceptable.

Detailed wiring rules, and delay formulas, are given in Application Bulletin No. 64-51-04B.

Power Requirements: +4v, 414 ma av., 828 ma max.
Dissipation: 1.65 watts av., 3.30 watts max.

Of the 52 pins on the module, all are individually connected to terminators except 16, 32, 48, 49, 51 and 0.





III. ACCESSORIES AND SERVICES

OTHER ESSENTIAL COMPONENTS OF A MODULE FAMILY

SDS offers a full line of T Series accessories, mounting hardware, and tools. They eliminate mechanical design cost, reduce procurement lead time, and reduce assembly time. SDS also offers a full range of services and documentation that save your engineering time.

Accessories include:

1. Cabinets with doors, optional side panels, ac power connectors, and optional swing-out mounting case containers (swing frames).
2. Individual 32-module mounting cases, and 3-case 90-module drawer; with hinged doors or fixed panels to cover mounting cases or to fill blank spaces.
3. Blower assembly for cooling.
4. Both compact and high-output power supplies.
5. Cable connectors and cables, and cable-plug modules. Both ribbon and coaxial cables are offered.
6. Spooled wire, cut-wire jumper kits, wiring tools, and individual module connectors.
7. Accessory modules for breadboarding and troubleshooting.
8. Indicator lamp.

These cost-reducing services and documents are provided:

1. Consulting engineering by experienced application engineers and by technically oriented sales engineers.
2. SDS designed and built special-order modules, made to your specifications at reasonable cost.
3. Application bulletins which give detailed, step-by-step instructions to help you design and build your system, all the way from system planning through logic design, assembly, wiring and documentation.
4. Data sheets on all products, which provide all technical details.
5. Logic sheets, on vellum, for all modules, to reduce logic design time, wire listing time, documentation time, and troubleshooting time.
6. Fast, off-the-shelf delivery of new modules or spares.
7. Module repair facility.
8. One-year warranty on all SDS products.

ACCESSORIES

Full specifications and detailed drawings of accessories are given in SDS catalog 64-51-15.

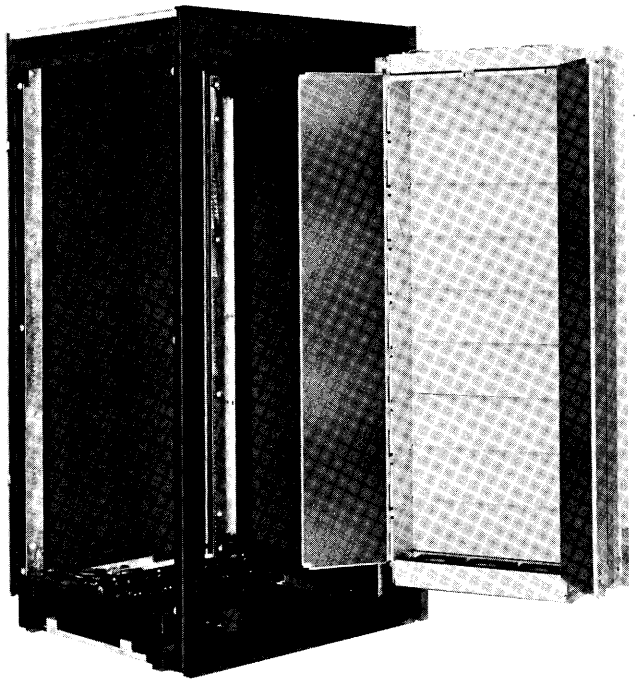
YT14, YT19 and YT24 CABINETS

Three types of cabinets are available, all with outside dimensions 63-3/8 inches high (including casters), 29-1/2 inches wide (without side panels) and 31-5/8 inches deep (with back door).

One cabinet, Model YT19, is made for mounting of individual 19-inch wide, 32-module mounting cases, power supplies and blowers. A vertical control panel is included. The cabinet also contains ac power outlets, a circuit breaker, a local/remote switch, dc wiring junctions and a power cord. Top and bottom have protective grills. Side panels (Model YT30) are optional. An insulated, soundproof hinged back door is standard.

A 24-inch version of this versatile system cabinet is available as Model YT24. The YT24 is ideal for use with 3-high and 7-high swing frames.

A third type, Model YT14, shown below, is designed to mount one or two swing frames which can each hold three, seven, or nine individual mounting cases, plus blowers. The swing frames contain the blowers, and also have front panel



covers in place for unused mounting case spaces. Double doors (shown open) completely enclose the mounting cases. Hinged back door, ac power sockets, and ac power cord are included in the YT14 cabinet. Side panels (Model YT30) are optional. Swing frame model numbers are YT43 (3-high), YT47 (7-high), and YT49 (9-high).

MT SERIES MOUNTING CASES

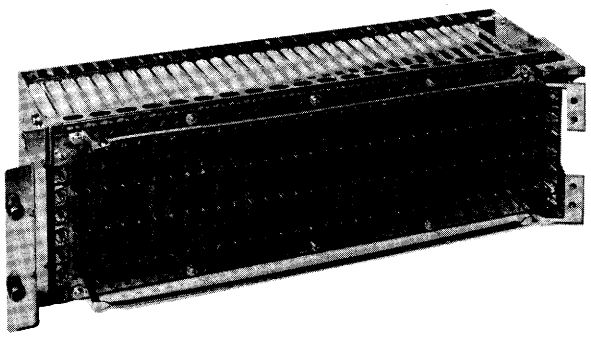
MT10, MT12, MT30, and MT32 Cases

Standard cases accommodate 32 modules, are 5.25 inches high, 7.90 inches deep, and fit into a standard 19-inch width rack. Wiring terminals are either solder tail or wire wrap. Each case comes with connectors, +4v and +8v power wiring, and ground plane installed.

Four combinations of fixed or hinged mounting, and the two pin types are available:

1. Solder terminals, fixed mount: MT10
2. Solder terminals, vertical hinge, right or left: MT30
3. Wire-wrap terminals, fixed mount: MT12
4. Wire-wrap, vertical hinge, right or left: MT32

All cases can be mounted with pins toward either front or back of cabinet. All brackets and hinges are adjustable and reversible, front-to-back and left-to-right. Cable troughs and pin protectors are standard on all mounting cases.



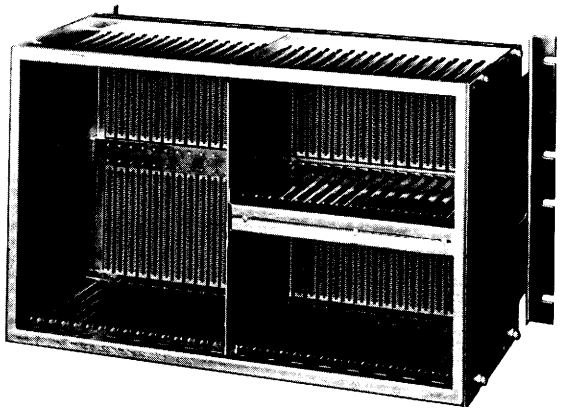
MT32 Hinged-Mount Case, Showing Ground Plane

MT13 and MT33 Cases

The MT13 (fixed mount) and MT33 (hinged mount) cases are similar to MT10/MT12 and MT30/MT32 cases, but are without the backplane/connector assembly. These cases facilitate combination of special equipment with T Series modules in the same assembly. The user provides his own connectors, ground and power bussing, etc.

MT42 Two-High Case

The latest addition to the SDS line of mounting cases is model MT42, designed to hold both double-height socket boards (ZJ14) and standard size modules, as well as the compact PT10 power supply.



MT42 Two-high Mounting Case

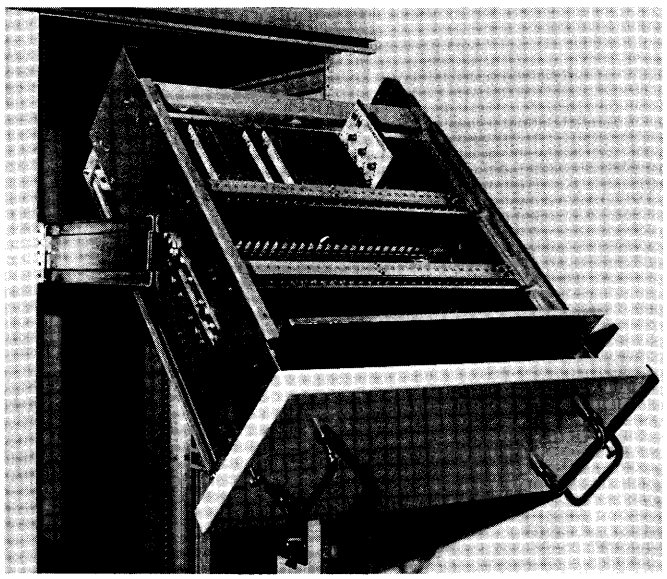
MTD1 and MTD2 High Density Cases

The MTD1 and MTD2 high density drawer-type mounting cases each contain three basic card cages with power and ground planes, identical to those used in the mounting cases described above, mounted in a drawer with tiltable slides which use ball-bearing rollers. Each case holds up to 90 modules, is 8.73 inches high, 22.03 inches deep, and fits into a standard 19-inch rack.

The slides allow the drawer to extend full depth from the cabinet and to be tilted in 45° increments over 180° from drawer-front point up, to pointing down.

A ZT20 blower with washable air filter is included. All power and ground connections to the three card cages are brought out to a terminal board. A module locking bar is provided for each card cage, and both top and bottom protective covers are furnished.

Panel mounted indicators and switches can be mounted behind the 1.09 inch deep front panel, which comes with two folding handles and captive fastening screws. The MTD1 case has solder-tail terminals while the MTD2 has wire-wrap terminals.



MTD1 High-Density Drawer Mounting Case

ZT SERIES DOORS

Three 19-inch wide hinged doors, reversible left or right, are available. Each door has a spring loaded latch at the end opposite the hinge. Indicator lamps, switches, meters, and connectors can be mounted in the doors.

Model ZT17	5-1/4 inches high (covers one MT series case*)
Model ZT18	10-1/2 inches high (covers two MT series cases*)
Model ZT19	15-3/4 inches high (covers three MT series cases*)

*except MTD1, MTD2, which have built-in front panels

Four 19-inch wide cover panels are also offered:

Model ZT40-1	1-3/4 inches high
Model ZT40-2	3-1/2 inches high
Model ZT40-3	5-1/4 inches high
Model ZT40-4	7 inches high

ZT20 BLOWER ASSEMBLY

The Model ZT20 Blower Assembly includes a housing which contains three 100 cfm muffin fans mounted side-by-side, three finger guards, a washable air filter, and mounting brackets. The entire assembly is 19-inches wide, 3-1/2 inches high, and 7-inches deep, and mounts with the fan blades turning in a horizontal plane. One ZT20 assembly delivers 300 cfm.

POWER SUPPLIES

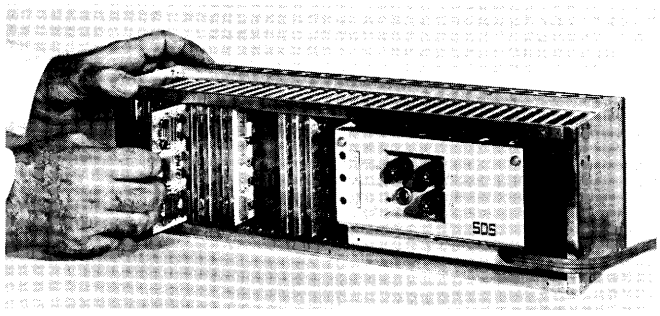
Model PT10 Compact Supply

Model PT10 fits into any MT mounting case, occupying 15 slots. It can power from 20 to 40 modules depending on load. Included are output voltage adjustments and protection against short circuits and overvoltage. Retainers are provided to lock the supply into the mounting case. The supply may be mounted in any position.

Input: 47 to 66 Hz, 1 ϕ, 100 vac to 230 vac

Outputs: +4vdc, 10 amp.
+8vdc, 2 amp.
-8vdc, 0.6 amp.
22 vac, 1/2 amp.
} Regulation: ±5%

Weight: 12 lb.

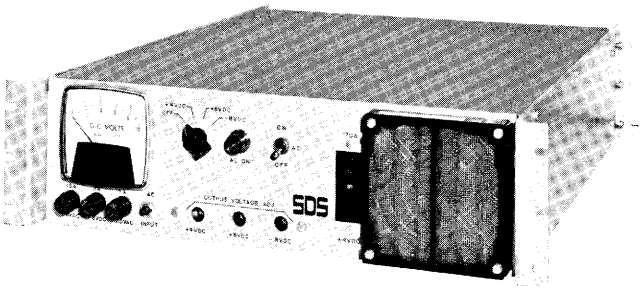


PT10 Compact Power Supply Installed Beside Logic Modules

Model PT12 High Output Supply

Model PT12 handles higher power applications. It occupies the full 19-inch rack width, is 5-1/4 inches high and 22-inches deep. Front panel has a cooling fan, a removable and washable air filter, an on-off switch, a multi-range switched voltmeter, and a pilot light. Included are output voltage adjustments, short circuit and overvoltage protection, and remote sensing. PT12 can power from 125 to 200 modules.

Input: 47 to 63 Hz, 1 ϕ, 115 vac, 127 vac, 208 vac, or 220 vac
Outputs: +4vdc, 60 amp.
+8vdc, 12 amp.
-8vdc, 4 amp.
25 vac, 4 amp.
(Regulation: ±5% on all outputs)
Weight: 100 lb.



PT12 High Power Supply

Models PT16, PT18, PT19 Large System Supplies

The PT16 supply provides logic power (+4v, +8v, -8v) in sufficient quantity to operate about 200 T Series modules. The PT18 provides higher voltages for use in peripheral or analog equipment: +25v, -25v, and +50v, as well as additional +8v. Both supplies draw their input, which is at 2,000 Hz, from the PT19 Inverter. The PT19 converts 60 Hz, 120 vac to 2,000 Hz, 120 vac. Use of the higher frequency permits lighter weight supplies at point of use and higher efficiency of distribution. The PT16 and PT18 both mount on the side of a swing frame. All supplies have overcurrent and overvoltage protection.

PT16 Specifications

Input:	2,000 Hz (±200 Hz), 1ϕ, 120 vac ±10% rms, regulated, modified square wave, at 10 amps. max.
Outputs:	+4.0 vdc (±0.2v) at 75 amp. +8.0 vdc (±0.4 v) at 40 amp. -8.0 vdc (±0.5v) at 5 amp.
Output load max:	600 watts

Output controls:	Margin switches for +10% and -10% steps, and ±10% output voltage control with potentiometer
Weight:	33 lbs.

PT18 Specifications

Input:	2,000 Hz (±200Hz), 1φ, 120 vac, ±10 rms regulated, modified square wave, at 5 amps. max.
Outputs:	+8.0 vdc, (±0.4v) at 8 amps. +25 vdc at 6 amps -25 vdc at 1 amp. +50 vdc at 1 amp.
Output load max:	290 watts
Output regulation:	±15% overall
Weight:	16 lbs.

PT19 Specifications

Input:	45 to 66 Hz, 1φ, 120 vac or 127 vac or 208 vac or 220 vac; 2,760 watts max.
Output:	2,000 Hz (±100 Hz) modified square wave, 120 vac, ±10% rms, regulated
Output load max:	1,200 va
Weight:	101 lbs.

PT23 and PT24 Digital/Analog Power Supplies

The PT23 and PT24 Supplies provide power for a typical 32-module analog chassis, such as the SDS MD51 Multiplexer-Digitizer, or the DA40 D-to-A Converter. Each consists of a PT10 logic voltage supply and a separate analog voltage supply, designed for compact 19-inch mounting.

PT23	PT24
Input (47-66Hz, 1φ)	
115 vac ±10%, 225 watts	115 vac ±10%, 570 watts
Outputs	
+4 vdc, 8 amp † +8 vdc, 3 amp -8 vdc, 0.6 amp } ±5% reg.	+4 vdc, 10 amp † +8 vdc, 2 amp -8 vdc, 0.6 amp } ±5% reg.
*50 vdc, 0.45 amp *50 vdc, 0.45 amp } unreg.	+25 vdc, 2.5 amp -25 vdc, 2.5 amp } ±0.5% reg.
+15 vdc, 1 amp -15 vdc, 1 amp } ±1% reg.	† Adjustable to 5 Volts for J Series Operation
* floating	
Weight	
50 lbs.	50 lbs.
Panel Height	
5-1/4 inches	5-1/4 inches

PT26 Analog Power Supply

The PT26 Supply consists of the analog supply portion of the PT23, but does not include the logic voltage supply section of the PT23. Specifications of the PT26 are:

Input: 47-66 Hz, 1 , 115 vac ±10%, 125 watts	
Outputs:	
50 vdc, 0.45 amp. (floating) 50 vdc, 0.45 amp. (floating)	unreg.
25 vdc, 1.2 amp. (floating) 25 vdc, 1.2 amp. (floating)	unreg.
Weight: 25 lbs.	Panel Height: 3-1/2 inches

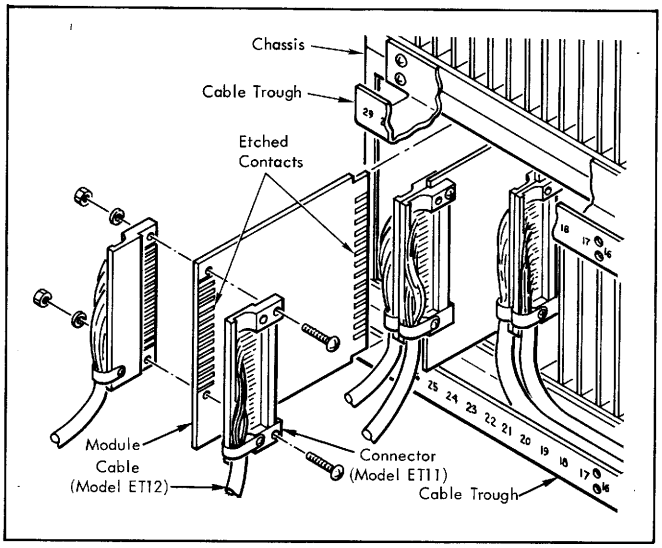
CABLING COMPONENTS

ET Series Coaxial Cabling Components

These coaxial cabling components minimize noise pickup and signal distortion, and simplify the mechanical aspects of cabling. The mechanical arrangement is shown in the diagram below. Each MT series mounting case has a cable trough attached to its bottom edge. Several fourteen-conductor 33 ohm coaxial cables (Model ET12) may be placed side by side in the trough. The shields and inner conductors of each cable are individually soldered to fourteen common ground points and fourteen independent signal points on a front-edge cable connector (Model ET11). Another ET11 Cable Connector is tied to the end of another cable and the two ET11's are bolted together, through holes in the front edge of an appropriately etched module. A pressure contact is made between the contacts on the ET11's and the module etch.

A preassembled cable-with-connectors assembly, using ET12 Cable and an ET11 Cable Connector at each end, is available as Model ET10-XX, where XX specifies the length of cable in feet.

A preassembled cable-with-connector assembly with an ET11 at only one end, using ET12 Cable, is available as Model ET14-XX-Y. Here, XX specifies length in feet and Y defines whether the ET11 is to be mounted on the etch side (normally left side) of a module or on the component side. Y=E for etch, C for component.



Cable Component Details

A Model ET13 Dummy Load must be placed at the end of a cable run to properly terminate the run. This item consists of an ET11 Connector which has fourteen 33 ohm resistors soldered between the fourteen ground and fourteen signal connection points.

Modules which are designed to accept ET11 connectors have front-edge contacts, twenty-eight on each side, fourteen connected together to ground and fourteen independent for signal connections. On most module types the ground and signal connections on one side are connected to corresponding etch connectors on the other side by plated-through holes. On some modules they are independent. Modules which have the front-edge contacts are: AT10, AT11, AT12, QT14, QT16, RT14, and ZT23 (described below). When ET11 Cable Connectors are attached, these modules cannot be located in adjacent module spaces, but a module of another type may be placed in the intervening slot.

ET32-XXXX Long Line Cable Assembly

The ET32-XXXX Long Line Cable Assembly is designed to be used in conjunction with a pair of AT52 Long Line Cable Driver modules and a pair of AT53 Long Line Cable Receiver modules to transmit 14 differential digital signals over lines up to 2000 feet long. For distances less than 200 feet use of AT10, AT11, and AT12 modules with ET12-XX Cable Assemblies is recommended.

The ET32-XXXX Long Line Cable Assembly consists of the following three sub-assemblies:

1) A center section of customer specified length of 15 twisted pair cable with a 32 pin male connector on one end and a 32 pin female connector on the other end.
2) A terminal section consisting of 35 feet of 15 twisted pair cable with a mating 32 pin female connector on one end and a pair of ET11 type connectors on the other end, and
3) A terminal section consisting of 35 feet of 15 twisted pair cable with a mating 32 pin male connector on one end and a pair of ET11 type connectors on the other end.

The ET11 type connectors are designed to mate the ET32-XXXX Long Line Cable Assembly to the etched connector on the outside edge of each of the AT52 and AT53 modules.

The ET32-XXXX Long Line Cable Assembly in conjunction with a pair of AT52 and a pair of AT53 modules provides a low cost transmission system with ±7 volts common mode rejection, capable of transmitting 1 Mhz bandwidth signals up to 1000 feet or 500 Khz bandwidth signals up to 2000 feet. The system has good immunity to crosstalk and externally injected noise. The pair of AT52 drivers send 14 complementary signals, having a starting differential amplitude of about 6 volts, along the twisted pair cables. Peaking filters following the drivers enhance the high frequency components which experience greater attenuation along the line. Signals received at the pair of AT53 receivers have differential amplitudes exceeding 2 volts after 2000 feet of travel. Terminating resistors on the AT53's prevent signal reflections.

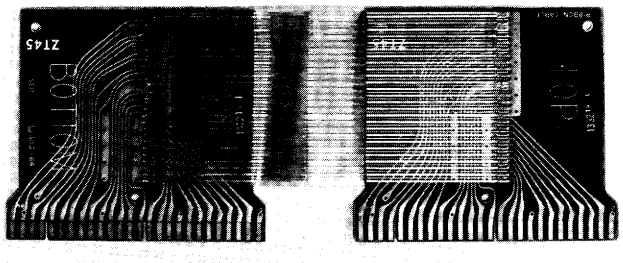
The system operates over the temperature range 5°C to 50°C. Electrical characteristics of the cable itself at 25°C are as follows:

Surge Impedance:	110 ohms -0%, +10%
D.C. Resistance:	25 nominal ohms per 1000 feet. (Single wire) wire size: 24 gauge.
Delay Time:	1.6 ± .025 nanoseconds per foot, each pair of wires.
Signal Rise Time:	115 ± 15 nanoseconds per 1000 feet, measured at the 10% and 90% amplitude points of the waveform.
Signal Fall Time:	190 ± 15 nanoseconds per 1000 feet, measured at the 10% and 90% amplitude points of the waveform.
Crosstalk:	With all but one pair of lines driven by a pulse having a 10 nanosecond rise time, the noise on the undriven pair shall not exceed 0.25 volt peak to peak at 1000 feet.
Dielectric Withstanding Voltage:	5000 VDC, from wire to wire.
Insulation Resistance:	100 Megohm minimum per 1000 feet, measured at 500 volts DC.
Maximum Dispersion:	400 nanoseconds at 2000 feet.

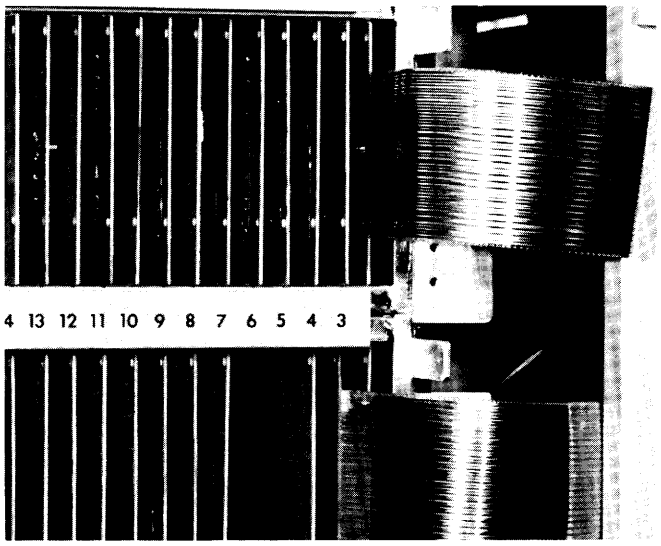
The center section of the long line cable assembly is manufactured to customer specified length. Each end section automatically includes 35 feet of cable. When ordering, the cable assembly should be designated as ET32-XXXX where XXXX specifies the required length of the center portion of the assembly in feet. Example: A long line cable assembly with a center section 240 feet long would be ordered as ET32-0240, and would reach drivers and receivers separated by a maximum distance of 240 feet + 70 feet = 310 feet.

ZT45 and ZT46 Ribbon Cable Assemblies

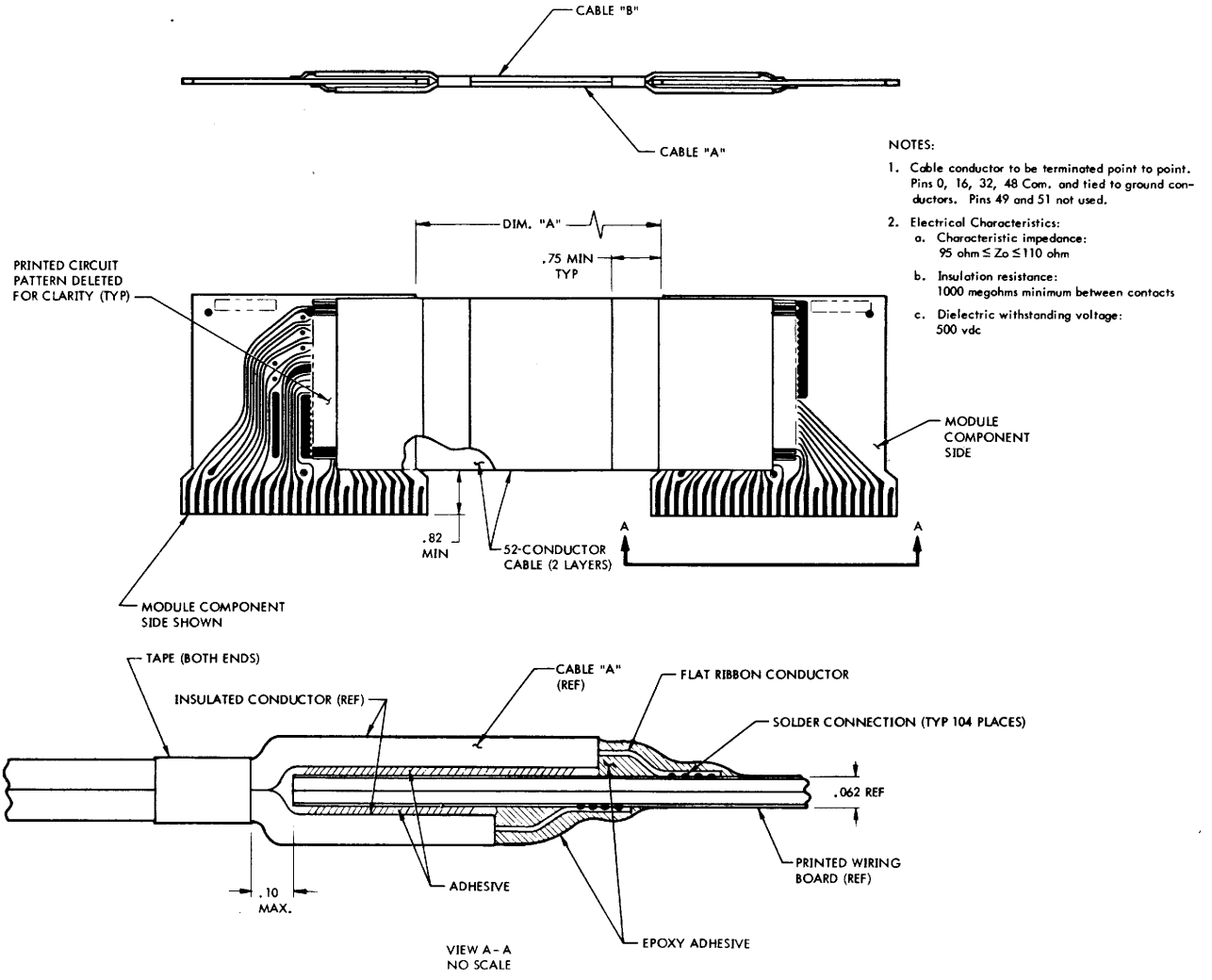
The ZT45 and ZT46 Ribbon Cable Assemblies use a flexible cable containing fifty-two copper foil conductors embedded in a durable ribbon of Teflon approximately 3 inches wide. Twenty-seven of the conductors are designated as ground conductors while twenty-five can carry signals, (although some are normally used as ground connectors also). The signal and ground conductors alternate across the width of the ribbon, with ground conductors at both outside edges.



ZT45 Ribbon Cable



ZT46 Ribbon Cable



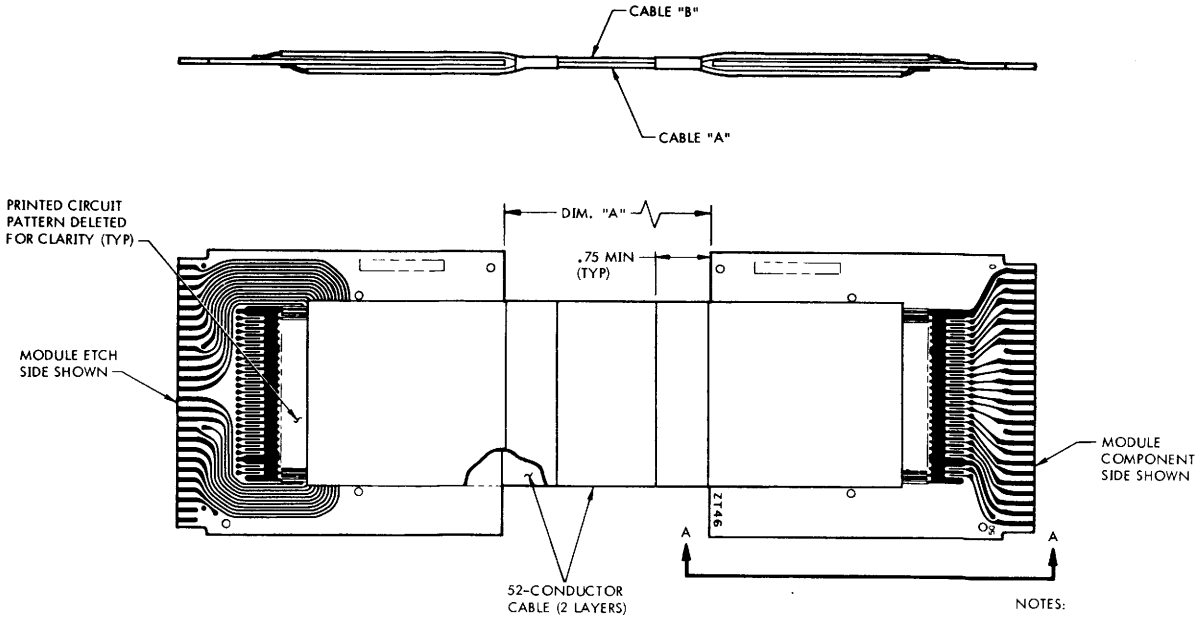
Assembly Drawing, ZT45

RIBBON CABLE STANDARD LENGTHS, ZT45 (VERTICAL)		
Length "A" in Inches *	Tolerance, in inches	Maximum dc resistance, in ohms
1.80	±0.05	1.0
7.00	+0.20 -0.00	1.0
12.70	+0.20 -0.00	1.0
18.40	+0.20 -0.00	1.0
23.70	+0.20 -0.00	1.0
28.90	+0.20 -0.00	1.2
29.90	+0.20 -0.00	1.2
39.50	+0.20 -0.00	1.5

Refer to Assembly Drawing, ZT45

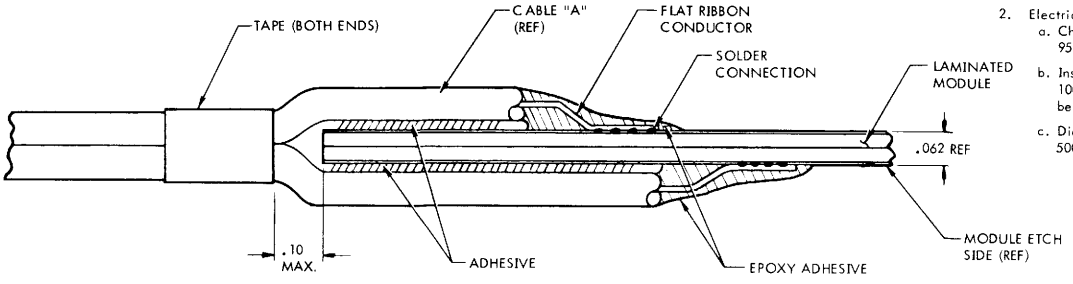
RIBBON CABLE STANDARD LENGTHS, ZT46 (HORIZONTAL)		
Length "A" in Inches *	Tolerance, in inches	Maximum dc resistance, in ohms
36	+1.0 - .0	1.4
44	+1.0 - .0	1.6
85	+1.0 - .0	2.7
100	+1.0 - .0	3.2
115	+1.0 - .0	3.5

Refer to Assembly Drawing, ZT46



NOTES:

1. Cable conductor to be terminated point to point. Pins 0, 16, 32, 48 common and tied to ground conductors. Pins 49 and 51 not used.
2. Electrical Characteristics:
   a. Characteristic impedance: 95 ohms ≤ Zo ≤ 110 ohms
   b. Insulation resistance: 1000 megohms minimum between between contacts
   c. Dielectric withstanding voltage: 500 vdc



VIEW A-A
NO SCALE

Assembly Drawing, ZT46

Two ribbons are always run in parallel; their edges are sewn together with nylon thread for handling convenience. This provides a total of 104 conductors per cable: Fifty-four ground conductors and fifty signal conductors.

The advantages of ribbon cable over coaxial are threefold. First, impedance is 100 ohms rather than 33 ohms, eliminating the need for special cable drivers and receivers for chassis interconnections up to 115 inches. Second, it results in a more compact installation with neater inter- and intra-cabinet wiring connections. Third, user can wire and test his mounting cases individually, then interconnect them with ribbon cable, rather than wiring across several adjacent mounting case back panels with logic wire.

Each cable assembly has a plug at both ends. The signal and ground conductors are soldered to the plug at appropriate points. The plugs are etched-circuit cards with laminated ground planes, identical in size and shape to SDS T Series and J Series modules. They plug into a slot in any SDS MT model mounting case.

In the ZT45 assembly the cable is connected to the plug at right angles to the plug's long axis, so that when plugged into a mounting case, the cable enters the case vertically, through a ventilating slot between modules. The ZT45 is designed for connecting signals between mounting cases stacked vertically in the same cabinet.

In the ZT46 assembly the cable is connected to the plug parallel to the plug's long axis, so that when plugged into a mounting case, the cable enters the case from the front. This assembly is most useful for routing signals between mounting cases at front and rear of the same cabinet, or between cabinets.

The cable may be folded for installation convenience. A great advantage of ribbon cable is that it may be clamped flat against the side of a cabinet and folded at 45 degrees to form a right-angle turn.

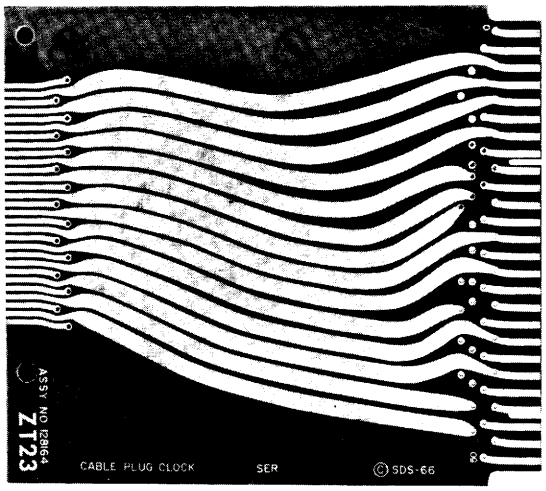
The ZT45 and ZT46 assemblies are offered only in standard lengths given in the tables on page 81. Lengths are measured from the edge of one plug to the edge of the other (identified as dimension "A" in the figure on page 81).

When ordering specify length in inches. For example, a ZT46 with an "A" dimension of 44 inches should be ordered as ZT46-44.

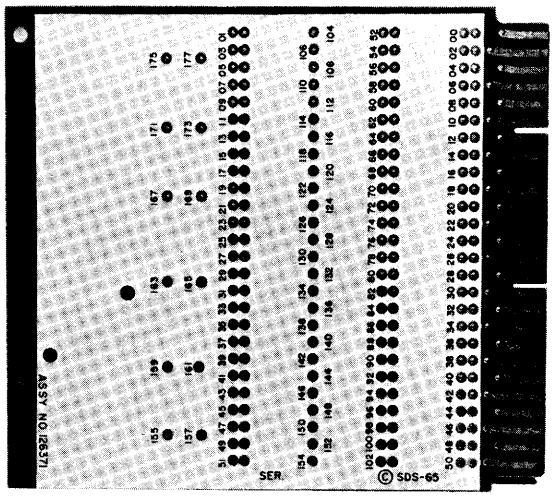
ZT15 and ZT23 Cable Plug Modules

Two cable-plug modules are available, the ZT15 and ZT23. The ZT23 Cable Plug Module accepts either one or two 14-conductor ET12 cables, connecting through ET11 connectors. The contacts on the two sides of the module are independent. Each side has a straight-through etched circuit pattern to take the signals from the cables straight to back panel pins.

The ZT15 Cable Plug Module performs the same function but does not have front-edge contacts. Instead, up to 44-shielded conductors can be soldered directly to the module. An etch pattern for adding passive decoupling components is also present on the board. The ZT15 is most useful for low frequency work (under 1 Mhz) where the effects of parasitics are not important.



ZT23 Cable Plug Module (Pressure Contacts)



ZT15 Cable Plug Module (Soldered Connections)

WIRING COMPONENTS AND TOOLS

ZT52 Logic Wire

The wire required for connection to back panel wrap terminals is a special type, with high tensile strength solid copper wire and a cut-proof insulation. The usual insulation, made from polyethylene or teflon, tends to cold flow over a period of time when placed under pressure such as exists when a wire is pulled tight against a wrap post. Eventually this causes intermittent short circuits which are extremely hard to find. SDS provides a 1,000 foot spool of wire, Model ZT52, for making wrapped connections. The same wire is suitable for soldered connections. In this case, however, a softer copper can be used since the wire need not grip the post.

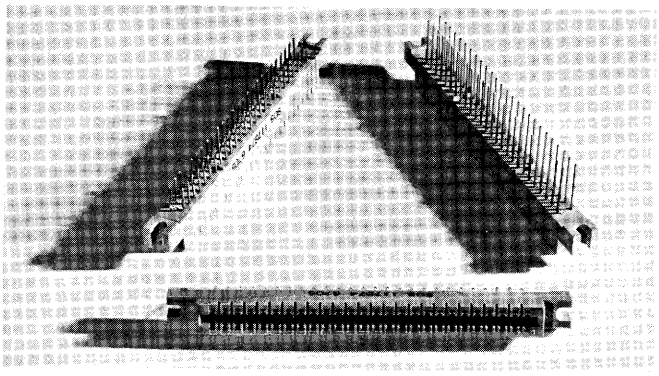
VT10 Jumper Kit

Model VT10 jumper kit contains an assortment of 500 slide-on jumper wires, primarily for use in systems whose wiring requires frequent change. This new approach offers significant improvements in reliability and convenience over taper pin techniques. The terminals at the ends of each wire slide on wire-wrap pins. Terminals may be stacked two high on each pin. Wire is No. 24 AWG insulated stranded copper. Wire lengths within each kit are:

Length	Quantity	Length	Quantity
1.0"	80	8.0"	20
2.0"	80	10.0"	20
3.0"	80	12.0"	15
4.0"	80	15.0"	10
5.0"	60	18.0"	10
6.5"	40	27.0"	5

VT11 and VT12 Back-panel Connectors

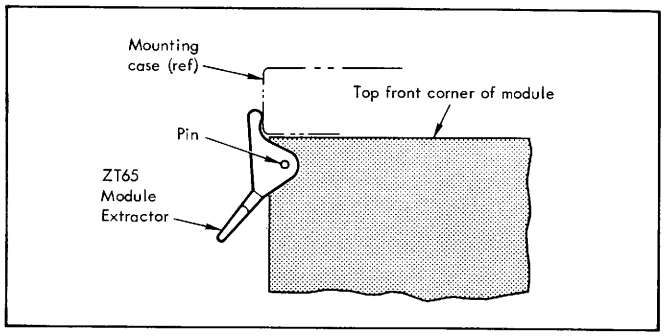
Model VT11 Connector with wire-wrap pins and Model VT12 Connector with solder-tails are provided for special module installations. They are identical to those used in the MT mounting cases.



VT12 (Solder tail) and VT11 (Wire-wrap) Connectors

ZT65 Module Extractor

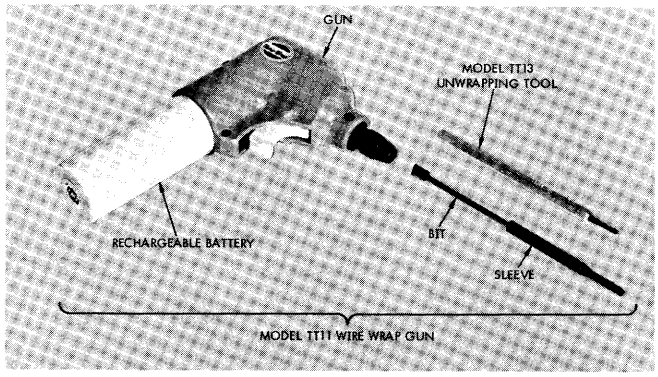
The ZT65 is a small plastic lever that mounts on any SDS module. It provides the mechanical leverage and bearing surface needed to make module removal simple and convenient.



ZT65 Module Extractor

TT11 and TT13 Wire Wrapping Tools

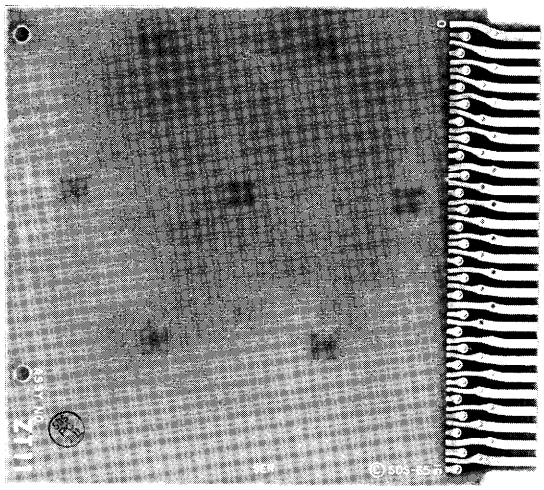
The Model TT11 Cordless Power Wire Wrap Gun, with bit, sleeve, and rechargeable battery is available, together with the Model TT13 hand-operated unwrapping tool, which is needed to remove improper wraps.



Models TT11 and TT13 Wire Wrapping Tools

ZT11, ZT37, ZT53 and ZT60 Accessory Modules

The ZT11 Blank Module has etched-circuit back-panel connectors. The remainder of the card is blank, for building circuits as desired.

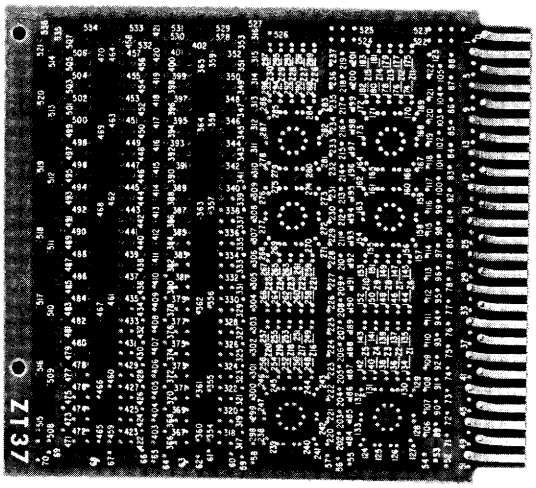


Model ZT11 Blank Module

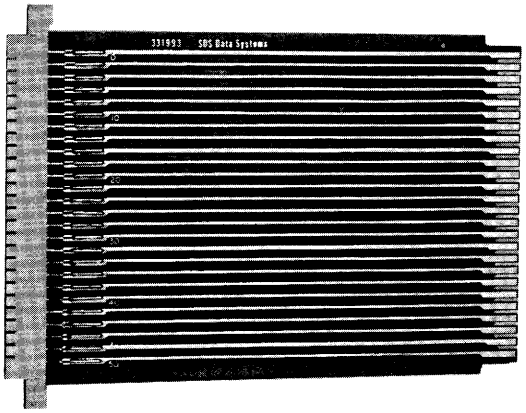
The ZT37 Breadboard Module (illustrated on next page) has a versatile etch circuit pattern arranged for convenient mounting of all standard components, including diodes, capacitors, resistors, transistors or IC's in TO-5 cans, flat packs, or the 14-lead dual inline package. This module permits custom building of special circuits while retaining the advantages and mechanical compatibility of T Series etch circuit construction.

The ZT53 Extender Module (illustrated on next page) has a straight-through etched circuit pattern and a VT12 connector mounted on its front edge. It permits the user to extend

any module in front of the rack so that circuit operation may be investigated while the module is plugged into the rack. Contacts are Rhodium plated for long life.



Model ZT37 Breadboard Module

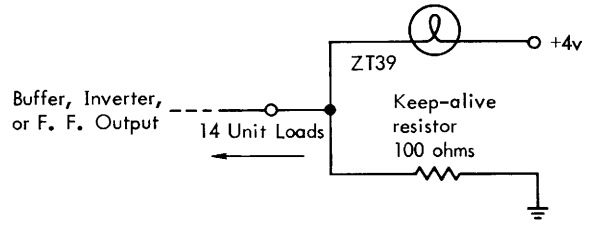


Model ZT53 Extender Module

The ZT60 Blank Module is similar to the ZT11, but has copper foil on both sides, for the production of custom etched circuits. Connector contacts are provided, already etched.

ZT39 INDICATOR LAMP

Model ZT39 miniature incandescent lamp mounts on a panel through a 9/32 inch hole with mounting clip provided. Wires can be soldered or wire-wrapped to the lamp. Any T Series standard 0v/+4v logic level output can drive the lamp, using the keep-alive circuit shown below to reduce turn-on current, protecting both driver and lamp.



SERVICES

AUTOMATED WIRING SERVICES

SDS utilizes in-house computer programs to generate fully documented wire lists from standard logic sheets completed by the customer according to his logic design. Digitally controlled machines wire the customer's mounting case back panel according to the computer generated wire list. Ask for Application Bulletin No. 8 for details.

APPLICATION ENGINEERING

Application Engineers and technically oriented Sales Engineers are available at regional offices to aid in specification writing, system planning, and preliminary logic design. These SDS engineers have considerable experience in the design of both small and large scale digital and analog systems. Typical recent applications include: specialized data processors to compensate for earth curvature, telemetry data converters, missile test sequencers, a digital phase meter, a digital control for a large data display, typesetting machine controllers, industrial process controls, data reduction from linear accelerators, medical research data processors, and interfacing units for SDS Sigma Computers.

APPLICATION BULLETINS

The detailed design work is necessarily performed by the module user. To familiarize the user and his assistants with T Series design rules, and to provide specific product information, SDS has prepared a series of fast-reading, self-teaching Application Bulletins, covering these topics:

No. 1: Back Panel Wiring Design
(Pub. No. 64-51-04)

No. 2: Multifunction IC Logic Module, Model FT19
(Pub. No. 64-51-05)

No. 3: Logic Design
(Pub. No. 64-51-06)

No. 4: Final Assembly and Wiring
(Pub. No. 64-51-07)

No. 5: Wire Lists and Documentation
(Pub. No. 64-51-08)

No. 6: Keyboard-Printer (Teletype) Interface
(Pub. No. 64-51-09)

No. 7: T Series Module Testers
(Pub. No. 64-51-10)

No. 8: Automated Wiring Service
(Pub. No. 64-51-11)

These bulletins contain tutorial information, step-by-step instructions, quantitative data, part numbers, pin numbers, and all other information that is necessary to get the job done quickly. The series is being continuously extended and other topics will be covered in future issues.

DATA SHEETS

Each customer is also given a full set of up-to-date data sheets covering all modules and accessories. Each sheet describes a product in detail. For example, the following data is given on each module:

1. Functional description, and theory of operation when necessary for a full understanding of the module.
2. Complete electrical specifications.
3. Application data (circuit connections, etc.) when necessary to fully utilize the module.
4. Logic diagram (input-output diagram).
5. Parts location diagram, with polarizing pins shown.
6. Replacement parts list.
7. Complete circuit schematic.
8. Other data if required.

LOGIC SHEETS

For a nominal charge the user is provided with pads of logic sheets for each module he buys. These sheets, which are described in Application Bulletin No. 5, can eliminate many hours of drudgery and also make it possible for the design engineer to delegate much of the wire-listing and checking activity to other technical or clerical personnel. Each logic sheet contains a logic diagram of the module, printed on vellum, and annotated where necessary with specific wiring hints.

SPECIAL MODULE DESIGN

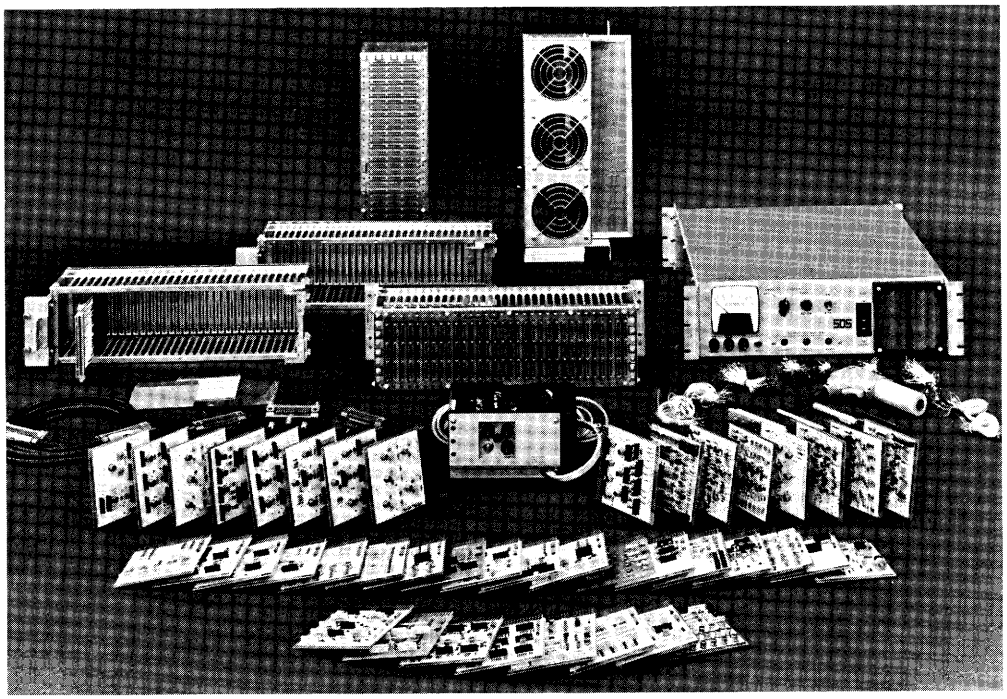
The SDS Engineering Department will design and build modules with special configurations of standard T Series circuits, or special supporting circuits, to customer specifications. Sometimes this approach leads to lower total cost, particularly when a large number of similar modules are required.

WARRANTY

SDS provides a one year warranty from date of sale.

OTHER REFERENCES:

1. "The Case For The Mixed Approach", Computer Design magazine, Sept. 1966
2. "The Ideal Logic Module Set", EDN magazine, March 1968
3. "Medicine For The Do-it-yourself Syndrome: Digital Modules", EEE magazine, April 1968



T SERIES PRODUCT INDEX AND PRICE LIST

Effective: 1 July 1969

QUANTITY DISCOUNTS

Order Exceeding	Discount	Order Exceeding	Discount
$ 5,000	3%	$ 50,000	10%
10,000	5%	100,000	13%
20,000	7%	200,000	16%
		500,000	20%

Discounts apply to single purchase orders placed and not subsequently altered in any manner by one customer specifying delivery and billing to single addresses.

SDS System Products Department
701 South Aviation Boulevard
El Segundo, California 90245

Model	Page	Description	Price
AT10	24	Cable Receivers	$150
AT11	24	Cable receivers/drivers	200
AT12	25	Cable drivers	100
AT22	25	Schmitt triggers	100
AT23	26	High current clock driver	120
AT24	27	Medium current clock driver	110
AT47	28	8-volt interface cable drivers	165
AT48	28	8-volt interface cable receivers	165
AT52	29	Long line drivers	100
AT53	30	Long line receivers	150
AT69	31	General purpose differential receivers	120
BT10	33	Buffered AND/OR gates	72
BT11	33	Buffered AND gates	80
BT12	34	Binary - to - octal decoders	97
BT13	34	Buffered matrix	100
BT18	35	Buffered AND gates	70
BT27	35	Buffered OR gates	75
BT31	36	Buffered AND gates	48
BT33	36	Dual-input 12-bit multiplexer	60
CT10	37	High frequency clock oscillator (1MHz to 10 MHz)	80①
CT16	37	Medium frequency clock oscillator (7.8 KHz to 2 MHz)	120①

Model	Page	Description	Price
DT12-1	38	4-bit D/A converters with buffers and reference	$ 60
DT12-2	38	4-bit D/A converters	45
DT13-1	38	6-bit D/A converters with buffers and reference	70
DT13-2	38	6-bit D/A converters	55
DT24	39	9-bit and sign D/A converter	160
ET10-XX	78	14 conductor cable with connectors	40②
ET11	78	Front-edge cable connectors	7
ET12-XX	78	14 conductor cable (per foot)	2
ET13	79	Cable dummy load	20
ET14-XX-Y	78	Cable assembly, single connector	30③
ET32-XXXX	79	Long line cable assembly	1000④
FT10	40	Basic flip-flops	92
FT11	41	4-bit high speed counter	76
FT12	40	Gated flip-flops	95
FT19	42	Multipurpose counters/registers	140
FT20	43	8-bit buffered latch registers	100
FT26	44	Buffered latch multiplexing matrix	80
FT27	45	Buffered latches	99
FT40	46	Fast access memory (128 bits)	480
FT43	47	Standard flip-flops	115
FT56	47	Clocked flip-flops	120

① Add $25 for each crystal. Specify frequency.

② $40 for basic assembly +$2 per foot of cable. XX defines cable length in feet.

③ $30 for basic assembly +$2 per foot of cable. XX defines cable length in feet. Define Y as C or E for connector mount on Component or Etch side of module.

④ $1000 for basic assembly +$1.50 per foot of cable. XXXX defines cable length in feet up to 2000 feet.

Model	Page	Description	Price
FT57	48	DC (RS) flip-flops	$ 55
FT58	48	10-bit buffered latch registers	125
HT58	49	Universal operational amplifier	170
HT72	51	Voltage comparators	79
HT73	52	Voltage comparators	120
IT10	54	Inverted AND/OR gates (AND/NORs)	72
IT11	54	Inverted AND gates (NAND gates)	80
IT13	55	Inverter matrix	100
IT14	56	Inverted AND/OR matrix (AND/NOR matrix)	70
IT18	57	Inverted AND gates (NAND gates)	70
IT27	57	Inverted OR gates (NOR gates)	75
IT31	58	Inverted AND gates (NAND gates)	48
KT10	58	Mercury-wetted relays	115
LT10	59	Logic elements (ANDs, ORs, NANDs)	80
LT11	59	Logic elements (AND/ORs, AND/NORs)	80
LT26	60	Switch comparators	120
LT50	61	Teletype send module (8-11 code)	350
LT54	61	Teletype receive module (8-11 code)	350
LT66	62	12-bit comparator	150
LT67	63	Fast full-adder	75
MT10	76	Fixed mount 32-module case, solder-tail	220
MT12	76	Fixed mount 32-module case, wire-wrap	150
MT13	76	Fixed mount 32-module case, w/o backplane, connectors	30
MT30	76	Hinge mount 32-module case, solder-tail	240
MT32	76	Hinge mount 32-module case, wire-wrap	160
MT33	76	Hinge mount 32-module case, w/o backplane, connectors	40
MT42	76	Two-high mounting case	300
MTD-1	76	Drawer type 90-module case, solder-tail	700
MTD-2	76	Drawer type 90-module case, wire-wrap	700
NT10	64	8v interface buffers	100
NT11	64	8v interface inverters	100
NT18	65	Negative logic to T Series interface (NORs)	55
NT19	65	Keyboard interface	100
NT33	66	T Series to negative logic interface	55
OT14	66	Adjustable one-shots (medium delay)	190
OT18	67	Adjustable one-shots (short delay)	120
PT10	77	Compact power supply	280
PT12	77	High output power supply	980
PT16	77	Large system logic power supply	1350
PT18	77	Large system peripheral and reference power supply	1000
PT19	77	60 Hz/2,000 Hz inverter	2500
PT23	78	Logic and analog power supply (50v and ±15v analog)	830
PT24	78	Logic and analog power supply (±25v analog)	830
PT26	78	Analog power supply	48

Model	Page	Description	Price
QT14	67	Lamp drivers	$100
QT16	68	BCD-decoder/drivers	90
QT17	68	BCD-decoder/indicators	120
RT14	69	Relay drivers	100
ST14	69	Manual toggle switches	120
ST41	71	Read only memory	150
ST44	70	Read only memory (diodes in place)	160
TT11	83	Cordless power wire-wrap gun	130
TT13	83	Manual wire-unwrapping tool	15
VT10	83	Jumper kit (500 wire)	125
VT11	83	Individual module connector, wire-wrap	5
VT12	83	Individual module connector, solder-tail	5
WT49	72	35v reference voltage regulator	190
WT53	73	25v reference voltage regulator	80
WT54	73	15v reference voltage regulator	80
XT10	74	Line terminators	30
YT14	75	24-inch computer add-on cabinet	750
YT19	75	19-inch system cabinet	1200
YT24	75	24-inch system cabinet	900
YT30	75	Side panel	100
YT31	76	Front door, blank	170
YT32	76	Front door with control panel	400
YT43	76	3-high swing frame	500
YT47	76	7-high swing frame	650
YT49	76	9-high swing frame	700
ZT11	83	Blank module	20
ZT15	82	Cable plug module (solder connection)	30
ZT17	77	19" wide hinged door, 5-1/4 inches high	40
ZT18	77	19" wide hinged door, 10-1/2 inches high	50
ZT19	77	19" wide hinged door, 15-3/4 inches high	60
ZT20	77	Blower assembly	80
ZT23	82	Cable plug module (pressure contacts)	25
ZT37	83	Breadboard module	20
ZT39	84	Indicator lamp	1.50
ZT40-1	77	Push-on panel, 1-3/4 inches	35
ZT40-2	77	Push-on panel, 3-1/2 inches	35
ZT40-3	77	Push-on panel, 5-1/4 inches	35
ZT40-4	77	Push-on panel, 7 inches	45
ZT45	79	Ribbon cable assemblies (vertical)	100
ZT46	79	Ribbon cable assemblies (horizontal)	100
ZT52	82	Logic wire (1,000 ft.)	60
ZT53	83	Extender module	40
ZT60	83	Copper-clad blank module	20
ZT65	83	Module extractor	25

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